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OPTIMIZATION STUDY OF HIGH POWER STATIC INVERTERS AND CONVERTERS

by Arthur B. Larsen and James E. Murray

Prepared under Contract No. NAS 3-2785 *by*
THOMPSON RAMO WOOLDRIDGE, INC.
Cleveland, Ohio
for

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Summary

This is the first quarterly report of the Optimization Study of high power static inverters for space applications. Work on the study began August 1, 1963. This report covers the time from August 1, 1963 to October 31, 1963.

The introduction outlines the goals of the study and the general program plan. The results of the first phase of study which involves determining specific program goals are included as the section titled "Methodology of the NASA Inverter Optimization Study." The second phase of the study which is only partially complete, is covered in sections on "Descriptions of Inverter Types" and "Hi-power 3200 cps Inverter Concept."

AUTHOR

INTRODUCTION

For space use, electrical power is utilized in the launch vehicle to provide guidance and control power so that the required velocity and directional accuracy can be obtained. In satellite applications electric power may be required for attitude control, navigation, guidance, communication and life support. Generally this electric power is derived from static sources of direct current. Static inverters and converters must be used to condition the DC power into forms which are acceptable for the final loads. Optimum utilization of these solid state devices for space applications requires detailed considerations of the application. These considerations include the performance requirements of the load, the regulation of the DC source, the method of inversion, the environment with its thermal considerations, weight restrictions, and the components themselves. Any method which attempts to optimize an inverter for space must be primarily concerned with three figures of merit. The first is efficiency because of the limited amount of power which is stored or generated and because reduced internal losses will reduce internal temperatures. The second figure of merit is the power to weight ratio. This is obviously important because of the thrust limitations of the launch vehicle. The last but certainly not least important figure of merit is the reliability of the inverter.

High performance static inverters and converters utilize nondissipative switching of high power semiconductors to achieve high efficiency and high

power to weight ratios. However, for space applications where it is usually impossible to carry spare units or to perform routine maintenance, the aspect of inherent reliability must be weighed against the performance goals, efficiency and weight to achieve the optimum mix. It is the purpose of this study to examine these various aspects of the space power conditioning problem in an effort to determine the most feasible techniques to fulfill the present and projected requirements for high power space static inversion equipment.

The power range to be examined covers the range of 100 watts to 10,000 watts, with frequencies from 400 to 3200 cps. Within these ranges there are many possible techniques which could conceivably be utilized. Furthermore, as new and improved semiconductor switching elements become available the possible number of techniques becomes even larger. However the performance goals of a particular application will restrict the possible choices of inversion technique. The first phase of the study, therefore, is an effort to determine with NASA a reasonable set of performance specifications for three or more projected applications. These performance specs are to be consistent with the reliable operation of an inverter which used advanced techniques to surpass minimum space requirements.

Having established these performance specs, the second phase of the study will be directed toward a selection of the most feasible approach for each projected application. In this phase the primary consideration will be a

selection of the power stage of the inverter. This selection involves a study of various techniques such as synchronous switching, high frequency pulse width modulation, etc. Integral with this selection of switching technique will be a choice of the switching element such as transistors, SCR's, gate controlled switches, saturable cores or hybrid combinations of the same.

The third phase of the study will be a combined analytical and experimental effort aimed at optimizing the components and circuitry for each selected approach.

The fourth phase will involve a re-evaluation of the selected approaches in light of the results of the analytical and experimental results. The result of this re-evaluation will be to make those modifications necessary for best program results.

The final phase of the study will consist of complete analytical evaluation of the finally selected approaches to determine their reliability, figures of merit and to illustrate the tradeoffs which exist between the various performance parameters.

The results of the first phase of this program, the establishment of the performance specifications, are given in the next section, (Methodology of the NASA Inverter Optimization Study.)

METHODOLOGY OF THE NASA INVERTER OPTIMIZATION STUDY

INTRODUCTION

The purpose of the overall study is to determine the best configuration of solid state inverters for space applications. To achieve this purpose the circuitry and the components, especially the switching elements, will be analyzed. However, the various performance parameters of the inverter and their interrelations with the components and the circuitry requires that certain ground rules be established. These ground rules will establish the method of evaluating the components and techniques so that the range of choice can be narrowed to a handful of selected approaches.

Categorization of Inverter Quantities

The quantities of primary concern in this study are listed below in three groups.

GROUP I Nominal Description of the Inverter

a) Full load volt-amperes (va) in a specified power factor range.

b) Frequency

c) Number of phases

d) DC input voltage

GROUP II Performance Specifications

a) Harmonic distortion

b) Variation of DC input voltage around nominal

c) High frequency transients on DC input

d) Output voltage

e) Output voltage regulation, steady state and transient

f) Output phase separation

g) Output short circuit protection

h) Overload capability

i) Unbalanced load capability

j) Output frequency regulation

GROUP III Parameters to be Optimized

a) Weight

b) Efficiency

c) Reliability

This list, while not all inclusive, does contain the quantities which are of primary concern to the electrical design of an inverter. They have been split into three separate groups. These particular groups were selected in conjunction with the proposed ground rules which are discussed below.

GROUND RULES

Group I determines the nominal requirements of the inverter. For this study it is proposed that these characteristics be limited to the following ranges for three inverter types:

GROUP I	TYPE A	TYPE B	TYPE C
Watt range	100 to 500 at 1.0 to .7 lag power factor	500 to 2000 1.0 to .7 lag power factor	2000 to 10,000 1.0 to .7 lag power factor
Frequency	400	400	3200
Number of Phases	3	3	3
Range of DC Input Voltage	15 to 100	15 to 100	15 to 100

The rationale for these choices are listed below:

1) Splitting the .10 Kw to 10Kw range into three parts allows the study to focus on the choice of best technique for each range. The use of a specific inverter technique, such as synchronous switching for instance, should be applicable throughout the selected range. The choice of components used in any inverter type would of course be selected to match the specific power under consideration.

2) The low end of the frequency band, 400 cps, was selected as the most appropriate frequency for the low and mid-power range inverters; 3200 cps, the top of the range, was selected for the high power inverter.

The intermediate frequency, 2000 cps, would undoubtedly use the same general technique as the 3200 cps inverter.

3) The range of 15 to 100 volts was selected as the probable limits of DC voltage sources that would become standard in the future. The selected inverter techniques will be capable of accepting a nominal (+10%, -20%) voltage within these DC limits without a change in the general configuration. As in the case of the power level ranges, the choice of specific components would be directly related to the DC voltage level under consideration.

Inverters which operate from DC sources of one volt and under are considered to be outside the main scope of this study. Studies indicate that this type of inverter is not especially suited for space applications because of its low power to weight ratio. Inverters which operate from high sources of DC voltage (1000 V DC and higher) are also outside the scope of this study. However, because of the low currents involved, this type of inverter offers a potentially high power to weight ratio if suitable switching techniques can be achieved.

The Group II performance specifications, which will hold equally for the three inverter types, are listed below.

Harmonic Distrotion:	Not to exceed 5% on total distortion with any sirgle harmonic not to exceed 2%
DC Input Voltage Variation:	+10%, -20%
High Frequency Transients on DC:	±200% of nominal for 10 microseconds or less
Output Voltage:	110/208 VAC
Output Voltage Regulation:	±2% for steady state, upper limit of transients during load switching to be + 50% of normal envelope with recovery to steady state in 20 cycles
Output Phase Separation:	120 ± 2 degrees
Short Circuit:	Automatic recovery to normal operation when short is removed
Overload:	200% for 5 seconds with ±4% regulation
Unbalanced Load:	Up to 1/3 the total maximum VA between highest and lowest phases

One additional area which is difficult to treat as an exact specification but is nevertheless important is the effect of the source. Solid state inverters use switching techniques to condition the raw DC power. This rapid switching causes the DC input current to contain AC components at multiples of the switching frequency. These AC components can cause transmission line disturbances as well as disturb the source itself. While these disturbances are essentially a detailed application problem, it is desirable to know approximately the time profile of the input current so as to ascertain the probable

magnitude of the problem. For each of the three inverter classes, the study will include the DC input current profile under the assumption that the source has negligible internal and transmission line impedance.

In the main body of this study the effect of varying these Group II specifications around their nominal points will be analyzed. If any of these specs appear to cause an undesirable change in the Group III parameters, they will be re-analyzed to show what can be done to maintain the best overall operation.

Group III, (weight, efficiency and reliability), represents those parameters which must be optimized for any specific mission. It will be the primary purpose of the study to select the methods and components which will allow a Group III parameter or parameters to be optimized for the given inverter types. These Group III parameters are usually inter-related in such a way that optimizing one of them will generally degrade the others. For instance, an extremely lightweight inverter might be designed by reducing the design margins on wound iron components. However, this would result in more heat loss in these components. This additional heat loss would reduce the efficiency and push the semiconductor components closer to their maximum operating temperatures thereby reducing reliability. The Group III parameters also interact with the Group II specifications. For instance, the lightweight inverter described above might also sacrifice harmonic distortion. These inter-relations between Group II and Group III as well as the interactions of the Group III parameters with each other will be analyzed in the later phase

of this study.

Both efficiency and weight are parameters that are easily measured. For this study the efficiency of an inverter will be defined as total AC power output (as measured at the load terminals) divided by DC power input. Total AC power output would include the power supplied by any harmonics remaining in the filtered output. The weight will be defined as the weight of the electrical components only. It will not include the weight of such things as heat sinks, outside case and other structural supports, connectors, etc. The weight of these additional items is closely related to the type of heat sinking that is available and the shock and vibration levels to be encountered. While it is beyond the scope of this study to determine the packaging configuration and hence total weight, a reasonable engineering estimate is that the weight of the electrical components will comprise 50% to 70% of the total weight in an aerospace type inverter.

The reliability of any inverter is obviously very important. However, the number attached to the concept of reliability is a quantitative expression of the effect of such factors as the number of components used to perform a certain function; the temperature, voltage and current stress on these components; the intrinsic reliability and failure modes of the componets themselves; and the number of redundant circuits or components that are used; and the required life of the mission. Most of the above information can be obtained from a theoretical analysis. However, the actual stress levels must be measured on breadboards etc., before a number can be assigned to the

actual circuit reliability. Moreover the temperatures of the components, especially the semiconductors, are a function of the packaging and cooling of the final unit. These factors combine to make any discussion of absolute reliability strictly an academic discussion if the stress levels existing in the final package are unknown. During the initial phases of this study the voltage and current stress levels can only be approximated by analysis and judgment based on the behavior of similar circuits. It will be this analysis and judgment together with the relative number of parts in the various circuits which will guide the selection of the techniques to be studied intensively. In the later phases of the study an absolute reliability analysis will be performed. This analysis will be based on voltage and current stress levels measured from available breadboards. The temperature of the components, especially semiconductors, will be assumed to remain within a specified band. The effect of radiation on the reliability of an inverter is beyond the scope of this study. However, in selecting the components, radiation of Van Allen Belt intensity will be assumed.

SUMMARY

The proposed ground rules categorize the various electrical quantities of the inverter into three groups: 1) Nominal Description: 2) Performance Specifications and 3) Those Parameters to be Optimized. This study will cover three nominal inverters - a low power 400 cps type, a mid-power 400 cps type and high power 3200 cps type. The technique selected for each of these

types will be applicable over a band of power and input voltage variation. The performance specifications for the three types will be identical. It will be the primary purpose of the study to select and analyze the techniques that will optimize the weight, efficiency and reliability, and simultaneously meet the performance specifications for each of the three types. A second purpose will be to study the interdependence of the specifications and the optimization parameters of the three types so that possible tradeoffs can be analyzed.

For these purposes, a general description of the operation, limitations, and advantages of the presently known inverter circuits is given in the next section, (Description of Inverter Types.) In addition, a detailed mathematical analysis is performed on two main types of inverter circuits used with silicon controlled rectifiers (SCR's) namely, the bidirectional series inverter and the McMurray Bedford circuit. These analyses are included not only to verify the results given in the general description of these inverter types and to indicate the techniques used in obtaining them but also, by presenting in great detail the operation of representative circuits, allow the reader to fully understand the complex sequence of operations which occur in SCR inverter circuits.

DESCRIPTION OF INVERTER TYPES

I INTRODUCTION

Solid state inverters are designed almost exclusively around two types of switching elements: silicon controlled rectifiers (SCR's) and transistors. The difference between these, of course, is the lack of ability to turn off the SCR at the gate; an external means must be provided to reduce the current in the SCR to zero. Provision must be made for this in all circuits using SCR's. In some circuits, this turn-off is an inherent part of the circuit; in others it is inherent for some load ranges, while in still others extra components must be added to provide this turn off. Series type inverter circuits (which are used almost exclusively with SCR's) are of the first two types. Parallel inverters (which are used with both SCR's and transistors) generally belong to the last class. Examples of these groups follow.

II SERIES INVERTERS

A. Unidirectional Series Inverter

A simple series inverter circuit with its waveforms is shown in Figure 1. Here, the SCR is gated on with a pulse. The current builds up through L, charging C. When C is charged up to the value E, the current in L is at its maximum and the voltage across L is zero. As L attempts to maintain the current in the circuit, the voltage across it reverses, charging C to a value greater than E. Thus by the time the current in L goes to zero, C has been charged up to a value considerably greater than

E, (2E in the no-load case) and the SCR is back biased and turns off. C now discharges exponentially through R, thus being readied for the next pulse. This circuit operates only for values of R above a certain minimum value, as obtained from the following mathematical analysis. The following discussion applies to the equivalent circuit of Figure 1 as shown in Figure 1-A.

The initial voltage on the capacitor is zero, and the closing of switch S_1 at t = o corresponds to the gating on of the SCR in the circuit of Figure 1.

The equations governing the operation of this circuit are:

$$i_1 = C\frac{dv}{dt} \qquad i_2 = Gv \qquad i_3 = i_1 + i_2 \qquad (G = \frac{1}{R})$$

$$\frac{di_3}{dt} = \frac{E-v}{L} = \frac{d}{dt}(i_1+i_2) = C\frac{d^2v}{dt^2} + G\frac{dv}{dt}$$

Rearranging terms, this equation for v can be put into the standard form:

$$C\frac{d^2v}{dt^2} + G\frac{dv}{dt} + \frac{v}{L} = \frac{E}{L}$$

with initial conditions $\begin{cases} v\big|_{t=0} = 0 \\ \frac{dv}{dt}\big|_{t=0} = 0 \end{cases}$

The solution for this if $\left(\frac{G}{2C}\right)^2 > \frac{1}{LC}$ (the overdamped case) is

$$v = E + \frac{\gamma_2}{\gamma_1}\left[\frac{E}{1-\gamma_2/\gamma_1}\right]e^{-\gamma_1 t} - \frac{E}{1-\gamma_2/\gamma_1}e^{-\gamma_2 t}$$

where

$$\gamma_1 = \frac{G}{2C} - \sqrt{\left(\frac{G}{2C}\right)^2 - \frac{1}{LC}} \qquad \gamma_2 = \frac{G}{2C} + \sqrt{\left(\frac{G}{2C}\right)^2 - \frac{1}{LC}}$$

It can be shown that, under these conditions that $V > 0$ for all finite t and that $dv/dt > 0$ for all finite t. Thus $i_3 = C\frac{dv}{dt} + Gv > 0$ for all finite t. Therefore, the SCR is always carrying current (i_3) and thus is always forward biased and never shuts off under these conditions. (Holding current, discussed in Appendix I, is neglected here.)

For $\left(\frac{G}{2C}\right)^2 < \frac{1}{LC}$, the solution for v is oscillatory, and given by $v = E - E e^{\frac{-Gt}{2C}} \cos wt - \frac{GE}{2Cw} e^{-\frac{Gt}{2C}} \sin wt$ where $w = \sqrt{\frac{1}{LC} - \left(\frac{G}{2C}\right)^2}$

The requisite condition for turn off of the SCR is that $i_3 = o$. This will occur for $-i_1 = i_2$ or $-C\, dv/dt = vG$. (The fact that i_3 must remain zero for a finite interval (as explained in Appendix I) will be neglected for simplicity.) The time at which $i_3 = o$ is the solution of the equation:

$$Ge^{\frac{Gt}{2C}} = \frac{1}{\omega L} \sin(\omega t + \tan^{-1}\beta)$$

where

$$\beta = \frac{4C\omega G}{G^2 - (2\omega C)^2}$$

Since the initial conditions fulfill these conditions, t = o is a trival solution to this equation. Whether or not another solution exists depends on the value of G. Figures 1B through 1E show plots of the two sides of this equation for various values of G. In Figure 1B, which is a plot for $\frac{2}{\sqrt{3}}\sqrt{\frac{C}{L}} \leq G \leq 2\sqrt{\frac{C}{L}}$, the fact that there is no solution in this region is obvious when one considers that:

1. Both curves start from the same point. (This is a result of t = o being a solution.)
2. The minimum slope of the exponential curve is greater than the maximum slope of the sinusoid, in the range under consideration.

From the diagram (Figure 1B) it is obvious that if the two curves intersect, it will have to be in the positive region of the first half sine wave. However, in this region, the maximum slope of the sinusoidal curve occurs at t= o and is given by:

$$\frac{d}{dt}\left[\frac{1}{\omega L}\sin(\omega t + \tan^{-1}\beta)\right]\Big|_{t=0} = \frac{1}{L}\cos(\omega t + \tan^{-1}\beta)\Big|_{t=0} =$$

$$= \frac{1}{L}\left[\cos(\tan^{-1}\beta)\right] = \frac{1}{L}\frac{1}{\sqrt{1+\beta^2}} = \frac{G^2}{2C} - \frac{1}{L}$$

The slope of the exponential is $\frac{d}{dt}\left[Ge^{\frac{Gt}{2C}}\right] = \frac{G^2}{2C}e^{\frac{Gt}{2C}}$ and has its minimum at the origin where it equals $\frac{G^2}{2C}$. Since $\frac{G^2}{2C} > \frac{G^2}{2C} - \frac{1}{L}$ for all finite positive L, the proof of statement 2 is established.

Figure 1C shows the two halves of the equation for $G = \frac{2}{\sqrt{3}}\sqrt{\frac{C}{L}}$. This is the value of G for which $\beta = -\pi/2$. For slightly smaller values of G than this, a solution still does not occur, (as shown in Figure 1-D),

but for still smaller values, a solution is finally reached (Figure 1-E). This is not a practical solution; however, because it does not take into account the time required for the SCR to turn off. From the complexity of even the simplified solution, which involves a transcendental equation, it should be obvious that the solution to the realistic problem is rather tedious.

Still smaller values of G result in practical solutions (1F). Note that once the curves intersect (i.e. $i_3 = 0$) the equivalent circuit of Figure 1A no longer holds; thus if the curve has two intersections, the second one is of no significance (the $t = 0$ intersection is not counted.)

Consideration of these results will indicate that the waveform drawings of Figure 1 are for the case of a very high resistance load; only as $G \rightarrow 0$ (or $R \rightarrow \infty$) does the capacitor voltage approach 2E.

B. Unidirectional Series Inverter With Load Switch

It is possible, through additional components, to disconnect R from the circuit during the charging period of C, thus allowing operation with any value of load. This scheme, shown in Figure 1G, is very simple, but the output waveform (which is the exponential discharge of a capacitor through a resistor) is dependent on load and of unidirectional polarity.

C. Bidirectional Series Inverter

Improvements on this circuit are shown in Figure 2. A detailed and mathematical description of the operation of this inverter is given in Appendix I. In this circuit R_L carries current in both directions as the capacitors are

alternately charged and discharged by SCR1 and SCR2. As shown in Appendix I, equations I-2c and I-9, the load and gate drive pulse frequency must meet certain requirements in terms of L & C in order for this circuit to operate; no-load or light load operation with this circuit is not possible. If driven at the proper frequency (refer to Figure I-8 and equation I-4), this inverter provides very nearly a sine-wave output for a constant load.

III PARALLEL INVERTERS

A. Simple Parallel Inverter

The basic parallel circuit is shown in Figure 3. Here the switching elements are shown as switches, since both transistors and SCR's are used in this circuit. For use with SCR's the components shown dotted must be included to provide for proper commutation of the SCR's.

The transistorized circuit puts out a square wave voltage into a resistive load; the output voltage of the SCR inverter, because of the resonant effects of L and C is a complex function of the values of L, C, the operating frequency, and the load. For the graphical presentation of the results of a steady state analysis of this type of inverter, the reader is referred to the literature "Parallel Inverter with Resistive Load," and "Parallel Inverter with Inductive Load," referenced in the Bibliography.

Unfortunately, these papers do not investigate the operation of the inverter under unloaded or switched conditions. It can be shown as follows that this inverter will not operate under no load conditions.

Consider any one half cycle of inverter operation. The equivalent circuit of Figure 3, under no load conditions, assuming S about to be closed is as shown in Figure 3A. If we assume that the SCR's are alternately gated on at a frequency ω_0 lower than the resonant frequency of the commutating components $\omega_c = \frac{1}{4\sqrt{LC}} > \omega_0$ then, at the time of the closing of S, there is no current in the circuit. When S is closed, the following differential equation applies to this circuit:

$$L\frac{di}{dt} + \frac{1}{4C}\int_0^t i\,dt = E + v_0$$

$$\begin{cases} i\big|_{t=0} = 0 \\ \frac{di}{dt}\big|_{t=0} = \frac{E+v_0}{L} \end{cases}$$

This has the solution:

$$i = 2\sqrt{\frac{C}{L}}(E+v_0)\sin\frac{t}{2\sqrt{LC}}$$

The solution, however, is only valid for $i \geq 0$, since S only conducts in one direction. Thus, this solution is valid only for $0 \leq t \leq 2\pi\sqrt{LC}$. During this time, the capacitor voltage changes from v_0 to

$$v_0 - \frac{1}{4C}\int_0^{2\pi\sqrt{LC}} i\,dt = v_0 - \frac{1}{4C}\int_0^{2\pi\sqrt{LC}} 2\sqrt{\frac{C}{L}}(E+v_0)\sin\frac{t}{2\sqrt{LC}}\,dt = -v_0 - 2E$$

Thus, in each half cycle, the equivalent capacitor (4C) voltage increases by $2E$, or the voltage on the actual capacitor C_c increases by $2(2E) = 4E$. Therefore, either the output transformer will soon saturate from the overvoltage or one of the SCR's will conduct, in either case resulting in a double fire or latch-up condition where both SCR's are conducting simultaneously. This is indicated in the waveform drawing of Figure 3B, where

the voltages are shown building up from the starting condition of $v_c = 0$. For very light loads, a similar situation occurs at start, except an equilibrium condition may eventually be reached if the voltage ratings of all the components are high enough. To handle inductive loads, the commutation capacitance C_c must be large enough to absorb the reflected load current for that part of the cycle during which the load is returning energy to the inverter (i.e. the load voltage and current are of opposite sign) without having the capacitor voltage rise to a destructively high value. This is also discussed in the literature previously cited in "Parallel Inverter with Inductive Load."

For an inverter which must operate over a wide range of (lagging) power factors, this can result in a considerable excess of commutation capacity at normal or light loads, giving rise to a condition similar to the no load case described. Thus, this type of inverter is not suited for general purpose applications where the load is of variable magnitude and power factor. This inverter, like all SCR parallel inverters also will not operate if the load impedance becomes too small. A detailed discussion of the reasons for this limitation in the case of the McMurray - Bedford circuit is found in Appendix II; the same reasoning can be applied to this configuration. Depending on the values of L, C, load, and operating frequency, an SCR which has been conducting may either be turned off by the attempt of the current in it to reverse its direction, or by the action

of the commutating capacitor in pulling the anode voltage of one SCR negative when the other SCR is first turned on.

B. The McMurray - Bedford Parallel Inverter

Improved operation of this circuit can be realized by the addition of so-called "reactive" diodes to provide a path for reactive currents which formerly went into the commutating capacitor (for the SCR circuit). This allows operation for all load power factors. The reactive diodes also serve to limit the voltages under no-load conditions, (the capacitor voltage is held to 2E) so that operation under no-load is now possible. The new circuit is shown in Figure 4, again, the additional parts required for an SCR inverter over a transistor inverter are shown. A detailed analysis of the operation of the SCR parallel inverter with reactive diode (the McMurray-Bedford circuit) is given in Appendix II. Waveforms of the SCR inverter at startup and steady state are given in Figures 10 and 11.

C_C is chosen according to equation II-15 to provide the desired minimum turn-off-time (e.g. 20 μsec) for the SCR's under the worst condition of commutating the maximum current at the minimum capacitor voltage. L_C is generally chosen to resonate with C_C at a frequency with half period approximately twice the turn-off-time. This is only a guide and L_C may be varied as desired, keeping in mind the following effects:

For a constant C_C, source voltage, and current to be commutated:

1. As L is decreased, the available turn-off-time is decreased,

because the commutating capacitor can be discharged more rapidly. Refer to equation II-29.

2. As L is decreased, the peak charging current to the capacitor is increased (equation II-2) although the average value (which determines the energy delivered to the capacitor) remains approximately constant; thus, the rms value of the current is increased, resulting in increased $i^2 R$ losses in the choke and output transformer.
3. As L is increased, the circuit is more affected by suddenly changing loads. A sudden increase in load currents results in a voltage developed across L in such a direction as to cause the commutating capacitor C_C to partially discharge into the load. If L is too large this effect can cause circuit failure upon load switching.

Because of the action of the reactive diodes in providing a path for reactive currents and limiting the capacitor voltage under light loading, this circuit will operate and start under a wide range of load magnitudes and power factors; however, should the load become too heavy, resulting in excessive currents at the time of commutation, then according to equation II-15, the circuit provided turn-off time is decreased and the inverter malfunctions.

C. Gate-Controlled Switch Parallel Inverter

Idealized waveforms for a transistorized or gate controlled switch (GCS) parallel inverter operating with a resistive load are shown in Figure 5. A typical GCS circuit is shown in Figure I-6. (Inductive loading will be considered later.) These are much less complex than those of the SCR

inverter as shown in Figure II-10 because of the absence of the commutating choke and capacitor from the circuit of Figure 5.

IV VOLTAGE REGULATION

The output voltage of all the inverters mentioned previously was a direct function of the d. c. input voltage and could be varied by changing this voltage. Rather efficient d. c. voltage regulators are now available; these could be interposed between the source and the inverter and controlled by the difference between the a. c. output and a reference to provide closed loop control of inverter output voltage.

A. Series Proportional D. C. Regulator

The simplest type of d. c. regulator (and the lightest, if heat sink requirements are not considered) is the series regulator, shown schematically in figure 5A and equivalently in Figure 5B.

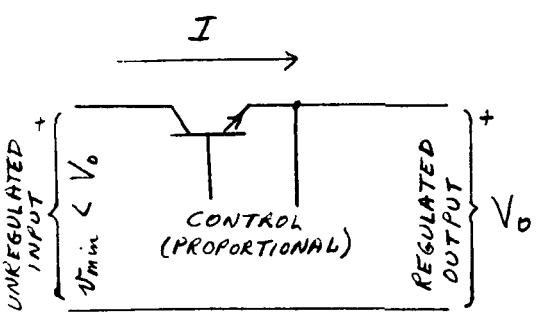


FIG. 5A
SERIES LINEAR REGULATOR

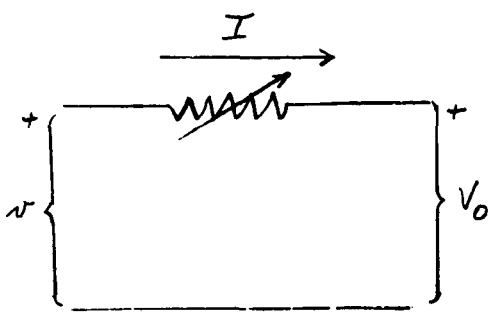


FIG 5B
EQUIVALENT CKT. OF FIG 5A.

For a load current I, the power input to the regulator (neglecting the power required by the low level control and sensing circuits) is VI, and the power

output of the regulator is $V_o I$. Thus, the maximum efficiency is $\eta = \frac{Po}{Pi} = \frac{VoI}{VI} = \frac{V_o}{V}$ Thus, for greatest efficiency, the output voltage should be as close as possible to the input. However, the regulated output can never be greater than the least value of the input; therefore, for any but small variations in voltage, this regulator becomes rather inefficient. Furthermore, the power lost in the regulator, $(V-V_o) I$, is all dissipated in the series control element which must then be adequately heat-sinked.

B. Series Switching D.C. Regulator

One of the first switching type d.c. regulator circuits used the same series transistor as the simple series regulator, but turned it full on or full off depending on how the output voltage compared with a reference. A simple LC filter smoothed out the large voltage variations caused by this switching, and a flyback diode was added to provide a path for the choke current during the periods when the series switch was off. The resulting circuit is shown in Figure 5C, and the waveforms in such a circuit in Figure 5D. The losses in this circuit are less than those of Figure 5A, for most cases and can be analyzed as follows:

Assuming a switching period of τ and a choke large enough so the current is approximately constant, the "on" time t_1 is approximately related to the period and the input and output voltages by the equation: $V_o = \frac{t_1}{\tau} V_{in}$ Therefore for a load current I_o, the losses in the circuit will be:

1. $I_o^2 R_4$ in the series choke

2. $I_o V_S \frac{t_1}{T}$ in the series switch

3. $I_o V_D \frac{(T-t_1)}{T}$ in the flyback diode

where V_D is the forward drop across the flyback diode, V_S is the forward drop across the series switching element and R_L is the resistance of the filter choke. It can be seen that these losses are independent of the input and output voltages. This is strictly true only for the case where $V_S = V_D$; otherwise the losses will vary slightly as the ratio of input to output voltage changes, because the time ratios t_1/T and $\frac{T-t_1}{T}$ will vary as this ratio changes. Thus, this circuit is suitable in applications where the input and output voltage of the regulator may differ by large amounts. Because of the choke, it is heavier (for a given current) than the circuit of Figure 5A, but this difference can be minimized by performing the switching at as high a frequency as possible (consistent with transistor switching losses) to reduce the choke size. Since this is a switching type regulator, it is also possible to use SCR's or GCS's in place of the transistor. With SCR's the circuits become more complex, again because of the necessity of having some method for turning the SCR off. A typical circuit (the Morgan Chopper) and its waveforms are shown in Figures 5E and 5F. The operation of this circuit is discussed in the literature.[6]

Both the transistor and SCR series type switching regulators provide an output voltage which can be no greater than the input.

C. Shunt Switching D. C. Regulator (Bedford Step-up Circuit)

The newly developed Bedford circuit shown in Figure 5G removes this restriction by providing an output not less than the input voltage.[9] It operates in the following manner; (refer to Figure 5G and the waveform drawing 5H). When S is turned on, current from the source builds up in L (and S). When S is opened, this current flows through D into C, charging it. The current in L then decays (because the output voltage is greater than input) until the switch (shown as a transistor in 5H) turns on again. While the switch is closed and current is building up in L, the load current is supplied entirely by capacitor C. With an input of V_i volts and I_i amps, and an output of V_o volts ($V_o > V_i$) and I_o amps ($I_o < I_i$) the average current carried by the switching element is $I_i - I_o$, and the average current carried by the diode is I_o.

Assuming an inductor resistance of R_L, diode drop of V_D and switching element drop of V_S, the losses in this circuit are then $I_i^2 R_L + (I_i - I_o)V_S + I_o V_D$. Again, this is independent of the input and output voltage to the same degree as the losses of the series switching inverter.

Figure 5-H shows the waveforms in the Bedford circuit for a step-up ratio of 2:1.

D. Inverter - Rectifier D. C. Regulators

Other circuits for d. c. regulation involve changing the d. c. to square wave a. c. with a simple parallel inverter, and then operating on this

a. c. with various types of modulators and rectifiers. Though more complex than the previous techniques described, this method is of advantage where the raw d. c. input is not near a value that can be readily used by the load; any desired amount of step-up or step down in voltage can be obtained with this technique by simply varying the turns-ratio of the inverter transformer. Since this incorporates inverter stages, which will be discussed in great detail later, and furthermore could not be advantageously used to provide a more optimum d. c. voltage level to drive an inverter (since it itself is an inverter and would have to work at the least optimum voltage), this method will not be discussed further.

E. Buck Boost D. C. Regulators

A modification of the above technique is the use of a square wave inverter-modulator-rectifier to provide only the difference voltage between the raw d. c. input and desired d. c. output. Its output is then connected in series with the d. c. input to provide the regulated output. The advantage of this system is that the inverter-modulator is required to pass only the error power instead of the total d. c. load. The output rectifiers still pass the full load current however, so the losses here are not decreased. The circuitry used in this technique is shown in Figure 5-J. This circuit can be designed to subtract from as well as add to the raw d. c. input voltage; if this is done, the maximum error power required is reduced by a factor of two, since the maximum output voltage of the regulator can be halved when its output can assume either polarity.

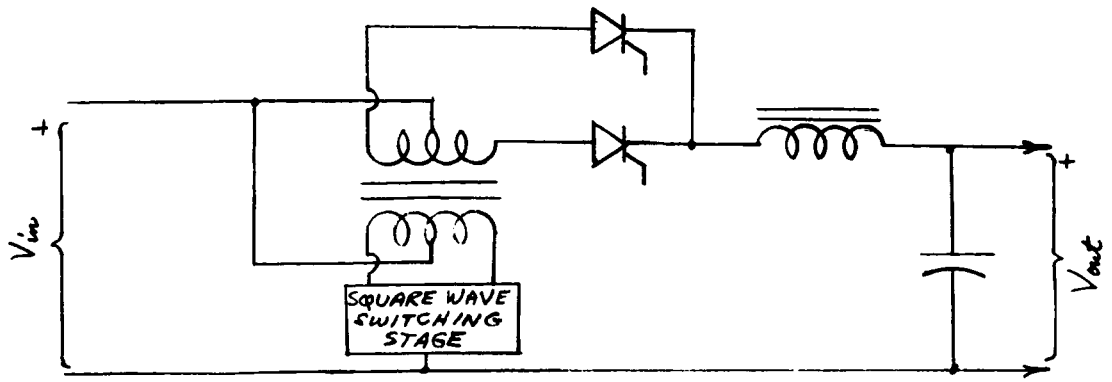


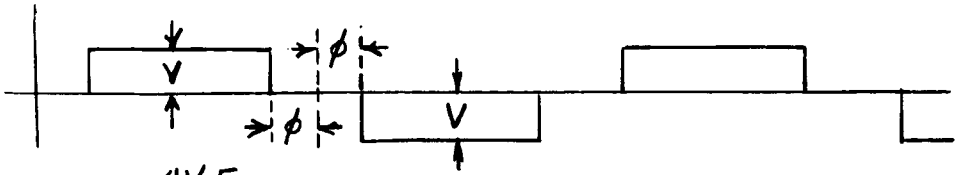
FIG. 5-J BUCK-BOOST D.C. REGULATOR

F. Quasi-Square Wave Regulation Techniques

1. Quasi-Square Wave Power Stage

Another method for voltage regulation involves increasing the complexity of the basic inverter circuit to provide for changing the output waveform of the inverter as required. One of the simplest outputs resulting from this is called a quasi-square wave and is illustrated below.

Harmonic analysis of the resultant wave (shown below) indicates the variation of the fundamental component of this wave with the dwell angle ϕ.



$$v(t) = \frac{4V}{\pi}\left[\sin\omega t\cos\phi + \frac{1}{3}\sin 3\omega t\cos 3\phi + \frac{1}{5}\sin 5\omega t\cos 5\phi + \cdots \frac{1}{2n-1}\sin(2n-1)\omega t\cos(2n-1)\phi\right]$$

Hence, by changing ϕ, the peak amplitude of the fundamental component of the above wave can be varied between $\frac{4V}{\pi}$ and 0.

With transistors and a resistive load this can be easily accomplished by only turning them on when an output is desired, instead of always having one on. This is indicated in the waveform drawings of Figure 5. When using SCR's the problem is more complex, since in all the circuits for parallel inverters discussed so far, the only way one SCR is turned off is to turn the other one on. Hence, in SCR inverters, additional circuitry is required to produce the output waveforms of Figure 5B.

2. Zero Clamping

Another problem which usually arises in the quasi-square wave inverter is that of providing a low impedance path for any secondary current flowing during those times when the output voltage is zero. This will occur when the load (as seen by the power stage) is inductive and is due to the effect of this inductance in maintaining a current flow after the driving voltage has been removed. The inductance may be caused by an inductive external load, or in the case of inverters with filters, will be the inductance of the filter. If a low impedance path is not provided for this current by some means, the voltage across the switches will rise in an attempt to maintain the current until the reactive diodes start to conduct. For reactive diodes connected as shown in Figure 4, this occurs when the total transformer primary voltage is 2E. (If there are no reactive diodes or other circuit elements to limit the voltage, it will continue to rise until it breaks over one of the switching elements, perhaps destructively.) The result is that the output waveform departs from the quasi-square wave (in a fashion dependent on the magnitude and phase of the load) resulting

in increased distortion and phase shift. An example of this is shown in Figure 5K for a resistive load with and without a tuned filter:

The first column of waveforms shows the waveforms obtained with a pure resistive load and no filter between the inverter output and the load. The waveforms obtained are what one would have expected: quasi-square waves. The second column shows what happens when the external load is still pure resistive but now a resonant series turned filter has been connected between the inverter output and load. The load current becomes approximately sinusoidal but the voltage at the secondary of the output transformer is no longer a quasi-square wave but a more complex wave with lower fundamental component and higher harmonic content than the one for the purely resistive load with no filter. Hence, any given filter will leave a higher harmonic content in the output with this input than with the quasi-square input.

For the case shown of the resistive load with filter, even through the output waveform is distorted, the fundamental component of this voltage still has the same phase relationship with the switch driving signals as does the output for the purely resistive load. However, should the external load be inductive, then the phase of the fundamental component of the output voltage will shift due to the fact that, during the "off" (or dwell) time, the change in the polarity of the output occurs not at the mid-point of the dwell period but at the time the output current crosses through

zero. Thus, the inverter output voltage during the dwell time will be non-symmetrical, resulting in a phase shift.

The problem of providing a path for transformed secondary current when neither of the power switches is on can be solved by a circuit such as shown in Figure 6. Here S_3 is closed whenever both S_1 and S_2 are open. Any secondary current in N_S is then transformed to the winding N_{sc} where it flows through S_3 with no appreciable voltage drop. Since there are no other voltage drops around the S_3 - N_{sc} loop, the voltage across N_{sc} remains low, thus keeping the voltage N_S low during the dwell period. Since current may flow through N_{sc} in either direction, S_3, when closed, must be capable of carrying a current in either direction.

3. Phase Shifted Square Waves

A quasi-square wave can also be generated by adding the outputs of two square wave inverters of variable phase difference, as shown in Figure 7. This method avoids the necessity of using an auxiliary switch to maintain low impedance during the zero voltage periods, since the internal impedance of the square wave inverter is always low. However, it does not make as full use of the transformer as the single stage generating a quasi-square wave, since in general at least part of the time the outputs of the two stages will be bucking one another, thus requiring a total transformer capacity greater than the load rating. Because, for part of each cycle (unless the two inverter stages are exactly in phase) one inverter

will be feeding energy back into the other one, both inverters must be equipped with reactive diodes.

4. Bridge Circuits

Better transformer utilization and lower switching element voltages (for a given supply voltage) can be obtained by using the bridge circuit of Figure 8. In this circuit, two switching elements are always closed at the same time. In this fashion the transformer is either connected across the d. c. supply or has a short placed across its primary to provide a low impedance, zero voltage output condition, as discussed earlier. With the bridge, the transformer has a single primary winding, all of which is used all the time, to produce either polarity of output or to be shorted to produce the zero voltage, zero impedance conditions. Depending on the times the switching elements are turned on, this circuit can produce quasi-square waves or square waves, as desired. The order of closing the switches in order to obtain a zero-clamped quasi-square wave output is shown in Figure 8. To produce square waves, S_1 and S_4 are closed and opened together, as are S_2 and S_3. In either case reactive diodes, as also shown on Figure 8, are necessary.

V HARMONIC REDUCTION

In general, the harmonic distortion of the unfiltered output of these switching circuits is too high for many applications. Two obvious solutions are to either filter the output to remove the undesired harmonics or

to use circuits which produce less harmonics. The optimum design is usually a combination of these two, since it is not too difficult to construct an inverter that suppresses the lower harmonics in the switching stages, and the higher ones are readily attenuated by simple filters.

A. Single Step Waveforms (Quasi-Square Wave)

The simple quasi-square wave, with $\phi = 30°$ has no third harmonic; three such waves each displaced by 120°, can be generated in a simple 3 phase bridge circuit as shown in Figure 9. This can provide a good start for a three phase inverter; however, holding ϕ at 30° (or any other fixed value) means giving up the voltage regulation capability of the quasi-square wave. Thus, some additional means is required for voltage regulation in situations where ϕ is held fixed for harmonic reduction purposes.

B. Multi-Stepped Outputs (Synchronous Switching)

Another method for reducing the distortion produced by the switching stage is to use a more complicated switching arrangement which is capable of providing intermediate values of output. Such a circuit is shown in Figure 10. Here the switches (either transistors or SCR's may be used) are closed in the proper sequence to provide the stepped waveform also shown in Figure 10. In this scheme, the switches farthest from the center tap provide the lowest output voltage, etc. Providing for reactive current in a scheme such as this can be a problem unless certain switches can be made bi-directional. It is also possible to produce such a waveform by adding a number of square waves of proper phase relationship in

a technique which is an extension of that shown in Figure 7. These more advanced switching techniques become more advantageous in multiphase inverters because several gating signals will be common to two phases; the control section for a three-phase multistepped inverter can be not appreciably more complex than that for a single phase unit. Voltage regulation in these more complex techniques may be obtained by a d. c. input regulator, by varying the width of some step in the waveform, or by adding together two such waveforms with a variable phase difference.

C. Constant Voltage Transformer Techniques

A combination of voltage regulation and harmonic suppression can be obtained through the use of special ferroresonant transformers designed for this purpose (e. g. the Sola transformer). These, however, have fairly high no-load losses and an output voltage somewhat sensitive to load power factor. They afford a very simple and reliable means of voltage regulation and harmonic suppression and also provide short circuit protection. When starting unloaded or operating under switched loads, they sometimes draw large spikes of magnetizing current; successful operation of an SCR inverter power stage under these conditions required a large commutation capacity when compared to normal demands.

D. Static Tap Changing

One technique of voltage regulation which can be useful under certain conditions is static tap changing. As shown in the diagram of Figure 10A, this uses semiconductors acting as switches S_1, S_2 .... to connect one of

several possible taps on the output transformer to the load. Two representative techniques for utilizing SCR's and transistors in a. c. (bidirectional) static switches are shown in Figure 10B. Which tap is selected will depend on the load and input voltage to the transformer. This technique has the advantage that it allows voltage regulation of a complex multi-stepped waveform without introducing distortion or phase shift as would be the case with a conventional on-off output modulator. This would be especially useful in a situation where the input voltage was very low so that an additional semiconductor in series with the input side (as would be the case with a conventional d. c. input regulator) would result in excessive losses, but where the output voltage of the switching stage transformer was high enough so that the drop in the static tap changing switching elements would represent a negligible fraction of the output power. The disadvantage is the large number of taps, and hence semiconductors required when either the d. c. input voltage to the power switching stage varies over a wide range (compared to the permissible variation in output) or the output voltage tolerance is so stringent that variations in output due to changes in load require a large number of taps.

E. High Frequency Techniques

SCR's could also be used to modulate a high frequency square wave to obtain a pulse-width modulated output like that of Figure 11. A block diagram of such a system, known as a cyclo-converter, is shown in Figure 12. Other techniques for low order harmonic reduction are the

various types of pulse modulation. The switched output and fundamental component of such a circuit is shown in Figure 11. These waveforms would be generated by circuits similar to those already discussed for square waves; the only difference being that the circuit is switched several times in each cycle. In these circuits; switching losses become much more significant, and components designed especially for high frequency use become a necessity. Figure 13 corresponds to a high frequency version of the quasi-square wave and can be generated by circuits similar to those used for the usual quasi-square waves. The advantage of the waveform of Figure 13 over that of Figure 11 is a further reduction in the amount of filtering required. At these high frequencies, it would also be reasonable to use a magnetic amplifier operating on a high frequency square wave to generate these waveforms.

The advantages of these high frequency techniques lie in the size and weight reductions possible both from high frequency operation and from the fact that the harmonics present in the unfiltered output are of a very high frequency compared to the fundamental, simplifying filtering. The main disadvantage is the increased switching loss. There is also presently a rather limited selection of semiconductors in the high-power high-frequency field. It might also be mentioned that unlike inverters of the quasi-square wave+ brute force bandpass filter design, which are restricted to sine-wave outputs, pulse width modulation inverters, which can efficiently use low-pass filters, are capable of providing any desired

waveforms with highest frequency harmonic below the cut-off of the particular filter used.

F. Passive Filters

Filters used for the outputs of the simpler inverter circuits generally consist of a series element (which is generally series resonant at the fundamental frequency) and a shunt path (which is capacitive at high frequencies and may be turned to parallel resonance at the fundamental frequency). The series section may also have impedance poles at those frequencies of greatest harmonic magnitude. The shunt section may likewise have impedance zeroes at appropriate harmonics. The basic filter concept is shown in Figure 14. In general, it is desirable to have the series element provide a low impedance path for the fundamental and a high impedance to harmonics. This first allows the fundamental current to pass without voltage drop from the inverter switching stage to the load, while the high harmonic impedance prevents harmonic currents from flowing in the switching stages, thus reducing dissipation. Similarly, the shunt path ideally presents an open circuit to the fundamental and a nearly short circuit to harmonic currents. (These harmonic currents may be the small amount that get through the series filter section, along with any due to load non-linearily.) As mentioned previously, pulse width modulation filters can be of the low pass type since the pulse width modulation waveform is essentially free of the lower order harmonics.

One proposed method for harmonic reduction in polyphase systems involves the use of a distributed transformer to couple the switching stage to the load. This can best be described as a wound rotor induction motor with locked rotor and having fractional pitch windings and skew selected to eliminated specified harmonics.

G. Active Filters

Another method of harmonic reduction is the use of active filtering. This involves using an error amplifier to make up the difference between the switching stage output and the desired sine wave output as provided by a sine wave reference source. A block diagram of such a system is shown in Figure 15.

Table 1 compares the various types of SCR inverters with respect to several parameters such as weight, efficiency, etc. These ratings are based on 400 cps inverters with 5% total harmonic distortion and operating at the 1 Kw level. This table shows that, in general, for fixed load operation, the series inverter is superior, but for large load variations, the McMurray circuit is favored.

Not yet complete studies comparing the McMurray inverter with transistorized power switching stages indicate that the losses in a silicon transistorized power stage would be approximately equal to those in the McMurray inverter, with the losses of a germanium inverter about 2/3 those of a silicon unit. The weights go in the same order, with the McMurray unit being the heaviest, the silicon inverter next and the lightest being the germanium.

TABLE 1

Comparison of Inverter Circuits

CIRCUIT	BI-DIRECTIONAL SERIES	SIMPLE PARALLEL	MCMURRAY, BEDFORD	MCMURRAY
PARAMETER				
Permissible Load Variations	3:1 max load changes	3: 1 max load changes	Operates from no load to full rated load	Operates from no load to full rated load
Inherent Voltage Regulation with Load Change	Poor	Fair	Good	Very Good
Efficiency	Circuit designed for fixed load 90% Circuit designed for 3:1 load change 70%	Same as Bi-directional Series	85% at rated load	90% at rated load
Weight (Inverter & Filter)	Fixed load circuit 15-20 lbs/KW 3:1 variable load circuit 35-45 lbs/KW	Fixed load circuit 18-21 lbs/KW 3:1 variable load circuit 25-30 lbs/KW	25-35 lbs/KW	23-27 lbs/KW
Control Circuitry	Simple	Simple	Simple	More Complex
Other Comments	Fail-safe under loss of drive	Not suitable for large variations in inductive loading		

Note: Portions of this table are taken from information presented in: "Quarterly Progress Report #4 on Voltage Regulation and Power Stability in Unconventional Electrical Generator Systems, prepared by General Electric for Bureau of Naval Weapons Contract NOw 60-0824-C, p. 69. (This table is based on operation at 400 ~, 28 VDC in, 115 V out, 1KW power level)

APPENDIX I - Analysis of the Series Inverter

As indicated in the introduction of this report, these analyses (Appendices I and II) serve three purposes:

1. Familiarization of the reader with the often-glossed-over finer details of inverter circuit operation.
2. Indication of the techniques used in inverter circuit analysis.
3. Verification of results stated but not proved in the earlier part of the report.

This appendix contains an analysis of the full-wave series inverter discussed in the body of the report. The circuit selected (See Figure I-1) was chosen as a simple representative of an important family of series inverter circuits.

The circuit of Figure 2 is shown again here for convenience (Figure I-2). The load is shown here as an actual resistance; in actuality, it would probably be the input impedance of some transformer coupled load. (The use of a transformer is possible here because of the a. c. nature of the output of this type of inverter.)

To start, assume that the supply voltage, E, has been applied but neither SCR has been gated on yet. Because of the voltage dividing effect of the capacitors C, the voltage at point Ⓐ (with respect to the ground point Ⓒ) will be E/2. Since neither SCR is on, point Ⓑ will also assume this potential, by virtue of its connection to point Ⓐ through R.

Now SCR 1 is gated on. This operation can be represented by the closing of switch S_1 on Figure I-2. The capacitor in Figure I-2 has a value of 2C and is connected to the ground side of the supply. This is a valid representation of the original circuit for purposes of computation of the current in R, L, and S_1 if the assumption is made that the supply source E has zero internal impedance; since, on an a. c. basis, the two capacitors C are effectively connected in parallel by the (zero a. c. impedance of the) d. c. source.

The equation for the current i_1 of Figure I-2 is given by the differential equation:

$$E = L\frac{di_1}{dt} + Ri_1 + v_o + \frac{1}{2C}\int_0^t i_1\,dt \qquad (I\text{-}1)$$

where t = o when SCR 1 is gated on. This is subject to the initial voltage condition of the capacitor. For generality, assume this has the value V_o. (In this special case of the first half cycle, we have $V_o = E/2$, where E is the supply voltage.) The voltage drop across the SCR has been neglected here; a simple and fairly accurate way to take this into account is to consider it as a fixed voltage drop of about 1.2 volts.

The solution to this equation is then given by

$$i_1 = \begin{cases} \dfrac{E-V_o}{2L\sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}}\left[e^{-\left(\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{2LC}}\right)t} - e^{-\left(\frac{R}{2L} - \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{2LC}}\right)t}\right] \\ \qquad \text{for } R > \sqrt{\frac{2L}{C}}\ ;\ t \geq 0 \qquad (I\text{-}2a) \\ \dfrac{E-V_o}{L}\,t\,e^{-\frac{R}{2L}t} \qquad \text{for } R = \sqrt{\frac{2L}{C}}\ ;\ t \geq 0 \qquad (I\text{-}2b) \\ \dfrac{E-V_o}{L\sqrt{\frac{1}{2LC} - \left(\frac{R}{2L}\right)^2}}\,e^{-\frac{Rt}{2L}} \sin\sqrt{\frac{1}{2LC} - \left(\frac{R}{2L}\right)^2}\,t \qquad (I\text{-}2c) \\ \qquad \text{for } R < \sqrt{\frac{2L}{C}}\ ;\ 0 \leq t \leq \frac{\pi}{\sqrt{\frac{1}{2LC} - \left(\frac{R}{2L}\right)^2}} \end{cases}$$

For the first two of these solutions, where $R \geq \sqrt{\frac{2L}{C}}$, it can be seen that $i_1 > 0$ for all finite $t > 0$. This means that once SCR 1 has been gated on it would, with an ideal SCR, continue to stay on because of the current i_1 always flowing in it. In practice, the SCR would eventually turn off when the current i_1 dropped below the holding current of the SCR. (Note: The holding current of an SCR is that value of forward current below which the SCR will revert to its non-conducting stage. It is typically around 20 milliamperes for present day medium and high current SCR's and varies considerably with temperature and between SCR's making operation in the region $R \geq \sqrt{\frac{2L}{C}}$ unsuitable for inverters, where the long waits required in such a circuit would necessitate impractically low duty cycles.)

However, the solution for $R < \sqrt{\frac{2L}{C}}$ is oscillatory, with a frequency of

$$\omega = \sqrt{\frac{1}{2LC} - \left(\frac{R}{2L}\right)^2} \qquad \text{or} \qquad f = \frac{1}{2\pi}\sqrt{\frac{1}{2LC} - \left(\frac{R}{2L}\right)^2} \tag{I-3}$$

The oscillatory condition means that the SCR will definitely be turned off by the circuit as the current attempts to reverse its direction. Starting with an initial voltage on the capacitors of E/2, then the current of the first half cycle as obtained from the previous general equations becomes

$$i = \frac{E}{2\omega L} e^{-\frac{Rt}{2L}} \sin \omega t \tag{I-4}$$

This holds for $0 \leq t \leq \frac{\pi}{\omega}$ which is the region

where $i \geq 0$.

This current flowing into the capacitor 2C of Figure I-2 results in a final voltage of:

$$v_f = v_o + \frac{1}{2C}\int_0^t i\,dt \qquad (I\text{-}5)$$

Evaluating this for the general case where the initial capacitor voltage is V, results in a final capacitor voltage (using the expression for current in the oscillatory case) of:

$$v_f = E + (E-V)\,e^{\frac{-R\pi}{2\omega L}} \qquad (I\text{-}6)$$

For an initial voltage of E/2, one obtains a final voltage of

$$v_{f_1} = E + \frac{E}{2}\,e^{\frac{-R\pi}{2\omega L}} \qquad (I\text{-}7)$$

at the end of the first half cycle which indicates a back bias on the SCR of an amount

$$\frac{E}{2}\,e^{\frac{-R\pi}{2\omega L}} \qquad (I\text{-}8)$$

Thus for natural commutation, (where the current in the circuit goes to zero of its own accord,) R should be less than $\sqrt{\frac{2L}{C}}$ ohms and the minimum time between the pulses applied to the alternate SCR's is given by

$$\tau \geq \frac{\pi}{\omega} + t_{t_o} \qquad (I\text{-}9)$$

where t_{to} is the turn-off-time of SCR1. (Note: Turn-off-time is defined as the time interval required for the gate to regain control of the unit after forward conduction has ceased).

On the next half cycle, the capacitors C, now charged up to a value somewhat greater than E, will be discharged by SCR 2 in a manner similar to the charging by SCR 1 (except the current direction is reversed and the initial condition different) with the result that the potential of point A will not end up at its t = o value. Since the circuit operates in a symmetrical fashion, in the steady state, the capacitor will end up being charged by SCR 1 to a voltage just as much above E as it is discharged by SCR 2 to a value below ground. Assuming that in the steady state the capacitor voltage prior to turning on SCR 1 has the value V_{ss}, then, after it has been charged by SCR 1, its voltage will be $E - V_{ss}$. The change in voltage is then $E - V_{ss}$ which equals v final $-v_o$ which from equation I-6 is:

$$\Delta v = E + (E - V_{ss}) e^{\frac{-R\pi}{2\omega L}} - V_{ss} = E - 2V_{ss} \qquad \text{(I- 10)}$$

The value for V_{ss} obtained by equating these two expressions for the change in capacitor voltage is:

$$V_{ss} = \frac{E}{1 - e^{R\pi/2\omega L}} \qquad \text{(I- 11)}$$

The "steady state" load current is then

$$i = \begin{cases} \frac{1}{\omega L}\left[\frac{E}{1 - e^{-R\pi/2\omega L}}\right] e^{\frac{-Rt}{2L}} \sin \omega t \\ \qquad \text{for } 0 \le t \le \pi/\omega \\ 0 \quad \text{for } \frac{\pi}{\omega} \le t \le T \end{cases} \qquad \text{(I- 12)}$$

where T is the period of the applied driving signal (which can be applied simultaneously to both SCR's since the one which conducted last will be back biased and hence not affected by a gating signal).

The current after SCR 2 is gated on at T is given by

$$i = \begin{cases} \frac{1}{\omega L}\left[\frac{-E}{1-e^{-\frac{R\pi}{2\omega L}}}\right] e^{-\frac{R}{2L}(t-T)} \sin \omega(t-T) \\ \qquad \text{for } T \le t \le T + \pi/\omega \qquad (I\text{-}13) \\ 0 \quad \text{for } T + \pi/\omega \le t \le 2T \end{cases}$$

where t = o is still the time of initial application of the driving pulse to SCR 1.

Thus, each cycle requires a minimum time of $\frac{2\pi}{\omega} + 2t_{t_o}$ where t_{to} is the turn off time of the SCR's. In general, the circuit is not designed for the turn-off time of each SCR, but rather to the maximum value that will occur in any SCR's used in the circuit. This value is around 20 μsec for selected high power SCR's and can run as low as 2-3 μsec for selected lower power SCR's. (Selection has generally been found necessary due to the fact that some SCR's have turn-off-times so high as to require impractically high values of commutating components.) This service is available from SCR vendors.

The load current i divides equally at the capacitors, 1/2 of it flowing in each capacitor. This results in currents throughout the circuit as shown in Figure I-3 (for SCR 1 on) and Figure I-4 (for SCR 2 on).

It can be seen that current is drawn from the supply on both half cycles, and that this current is equal to only 1/2 the load current. This is the reason for connecting the load capacitor as shown in Figure I-1 instead of the method shown in Figure I-5. Analysis of the circuit of Figure I-5 will show that it possesses the same equivalent circuit as far as the load resistance is concerned, namely that of Figure I-2. Hence, the solution for the current i of Figure I-5 will be the same as that obtained previously for Figure I-1. However, Figure I-5 will pull a current pulse i_1 from the supply when SCR 1 is gated on and will not affect the supply at all when SCR 2 is turned on; the discharge path (i_2) does not include the d. c. supply. Thus, this latter scheme (Figure I-5) puts more ripple on the supply to accomplish the same job as the scheme of Figure I-1 and hence is not as desirable.

It can be observed from these equations the effect of the load resistance on whether or not the circuit will operate (eq I-2a, I-2b, I-2c) and, if it does, its natural resonant frequency (eq. I-3) and output voltage (eq. I-11). This indicates one large disadvantage of the series type inverters; their dependence on the load. This, of course, would not be a problem with a fixed load since the circuit parameters can be selected to allow operation with any predetermined load.

The discussion so far has been developed on the basis that SCR 2 is not gated on until SCR 1 has ceased to conduct and has been back-biased for a period at least as long as its turn-off-time. The situation when this condition is not

met; (i.e. when SCR 2 is turned on before SCR 1 has ceased conduction) will now be investigated.

The circuit (Figure I-1) is assumed to be operating in a steady state mode where the potential of point Ⓐ varied from V_{ss} to $E-V_{ss}$. In the previous discussion, the value for V_{ss} was derived for the case of natural commutation (eq. I-11) and it could be seen that the value was always negative. For this discussion this value cannot be used because the conditions under which it was derived no longer hold. However, a limit on the value can be obtained by a simple argument. Suppose the steady state value for V_{ss} was greater or equal to E/2. Since, by the symmetry of the circuit the maximum and minimum of the potential at point Ⓐ must be equidistant from the value E/2, and since the maximum (which results from SCR 1 being gated on) must be greater than the minimum (V_{ss}, which results from SCR 2 being turned on) V_{ss} must be less than E/2.

Referring again to Figure I-1 and assuming the two halves of the center tapped inductor to be perfectly coupled, then with SCR 1 on, the voltage at E (the anode of SCR 2) must be equal $V_e = E - 2L\frac{di}{dt}$. Substituting the value for i (eq. I-2c), into this equation for V_e results in

$$V_e = E - 2(E - V_{ss}')\left[e^{-\frac{Rt}{2L}}\cos\omega t - \frac{R}{2\omega L}e^{-\frac{Rt}{2L}}\sin\omega t\right] \quad \text{I-14}$$

Since $V_{ss} < E/2$, V_e is negative at $t = 0$; however, at some time before $t = \frac{\pi}{\omega}$, V_e will go positive. If a pulse is applied to SCR 2 before its anode

is positive, nothing will occur. If the gate is maintained in the on condition, then when the anode attempts to go positive, (which will occur when the center tap of the choke reaches E/2) it will be held to ground potential by SCR 2, and the current in the inductor will continue to rise at a rate of E/2L amps/sec. This will keep both SCR's on, creating a fault condition. Therefore, having the gate of SCR 2 on as the anode of SCR 2 goes positive will result in a circuit malfunction.

However, let us now assume that SCR 2 is off until point A just exceeds a potential of $E/2 + iR$ by an amount Δ. Figure I-6 shows the potentials and currents in the circuit at this time (before SCR 2 is turned on). Immediately after SCR 2 is turned on, the voltages and currents are as shown in Figure I-7. These are obtained from the previous values using the facts that:

a) the capacitor voltage cannot change instantaneously.

b) The current in the inductor cannot change instantaneously, although it may transfer from one winding to another.

Thus, by turning SCR 2 on, SCR 1 has been back-biased. Hence SCR 1 has been commutated without waiting for the normal time of a half cycle at the circuit resonant frequency ω. (For simplicity, the fact that this back-bias must be maintained for a period at least equal to the turn-off time of SCR 1 has been neglected.)

We have thus shown that under certain conditions one SCR may be turned on

APPENDIX II - Analysis of the Parallel Inverter

This appendix contains an analysis of the McMurray - Bedford parallel inverter circuit shown in Figure II-1. As was done for the series inverter in Appendix I, analytical expressions are obtained for the voltages and currents in different parts of the circuit. The effect of load on circuit operation is indicated, as well as the action of the reactive diodes.

This analysis is carried out for the circuit of Figure of II-1, again using SCR's since the mechanism of commutation in this circuit is different from that of the series inverter. Furthermore, since the parallel inverter has a square wave output (unlike the nearly sinusoidal output possible with the series inverter) a filter is generally necessary. Since this modifies the operation of the inverter somewhat, the analysis was performed for the inverter with a filter. The filter will be assumed ideal in the sense that it presents an infinite impedance to all harmonics of the inverter output but passes the fundamental without loss or phase shift. The generalized load impedance is:

$$Z_L = |Z_L| \angle \theta$$

A 1:1:1 ideal transformer is assumed, with taps at a fraction K of each of the primary windings as shown. Again, at t = o the capacitor is uncharged and both SCR's off. When SCR 1 is turned on, the equivalent circuit becomes that of Figure II-2, which can be further simplified to that of Figure II-3. This transformation from Figure II-2 to Figure II-3 requires the assumption that the transformer of Figure II-2 is ideal and thus transforms the capacitor C

before the other has been naturally commutated off without causing a circuit malfunction. This fact could be useful in operating a series inverter at its maximum natural frequency with a slightly varying load; it says that even though a load change might result in a somewhat lower natural frequency than the inverter drive source provides, operation is still possible. The load current and SCR anode voltage for the three representative relationships between the driving frequency and natural resonant frequency are shown in Figure I-8.[4] According to the literature, it is also possible to operate in the over damped regions (equation I-2a, I-2b) in this mode; this was not investigated at this time.

by the square of its turns ratio from the C of Figure II-2 to the $2^2C = 4C$ of Figure II-3. Because the filter allows only fundamental current to flow, the high frequency of the initial charging current i results in its being effectively decoupled from the load during this first switching interval.

The equation for the current in this circuit (Figure II-3 is)

$$L\frac{di_1}{dt} + \frac{1}{4C}\int_0^t i_1\,dt + \frac{v_o}{2} = E \qquad \text{(II-1)}$$

subject to the intital conditions

$$i_1\big|_{t=0} = 0 \qquad v_c\big|_{t=0} = v_0 \quad \therefore v_{4C}\big|_{t=0} = \frac{v_0}{2}$$

For a general solution, it has been assumed that an initial voltage of V_o is present on the capacitor of Figure II-2 (or an initial voltage of $V_o/2$ on the capacitor of Figure II-3). In the specific case of the first half cycle, V_o will be set equal to zero in the general solution.

This has the solution

$$i_1 = 2\left(E - \frac{v_0}{2}\right)\sqrt{\frac{C}{L}}\sin\frac{t}{2\sqrt{LC}} \qquad \text{(II-2)}$$

This equation is valid only when $i_1 \geq 0$ (because the SCR can be represented by a closed switch only in the region where it is carrying forward current) which holds for

$$0 \leq t \leq 2\pi\sqrt{LC}$$

During the period when SCR 1 is conducting, the capacitor 4C will be charged up by the current i to a value $\frac{v_c}{2}(t)$ (where V_c is the voltage across the actual capacitor C) which is given by the equation:

$$\frac{v_c}{2}(t) = \frac{v_0}{2} + \frac{1}{4C}\int_0^t i_1\,dt \qquad \text{II-3}$$

Again, this is a general expression for $\frac{v_c}{2}$ for arbitrary values of V_o; as before, for the special case of the first half cycle, we will set $V_o = 0$.

Because of the presence of the reactive diodes (D_1 and D_2) the voltage across the capacitor cannot rise to more then 2E/K, since if it did, it would require

that one of the diodes would be forward biased. Thus, what happens is that the current i_1 flows into the capacitor until the capacitor voltage equals 2E/K; the current then flows in the reactive diodes. This is shown on the waveform drawing of Figure II-10 which shows the startup and steady state operation of this inverter with a resistive load.

Substituting the known value for the current (eq II-2) into the general equation II-3 for the capacitor voltage results in an explicit expression for $\frac{v_c}{2}$:

$$\frac{v_c}{2} = \frac{v_o}{2} + \frac{1}{4C}\int_0^t i_1 dt = \frac{v_o}{2} + \frac{1}{4C}\int_0^t 2\left(E - \frac{v_o}{2}\right)\sqrt{\frac{C}{L}}\sin\frac{t}{2\sqrt{LC}}dt \qquad \text{(II-4)}$$

$$= E - \left(E - \frac{v_o}{2}\right)\cos\frac{t}{2\sqrt{LC}}$$

Equating $\frac{v_c}{2}(t)$ with the maximum value of $V_c/2$, namely E/K; one obtains the equation for the time τ_2 when the maximum voltage is reached:

$$E - \left(E - \frac{v_o}{2}\right)\cos\frac{\tau_2}{2\sqrt{LC}} = E/k \qquad (k \le 1) \qquad \text{(II-5)}$$

Therefore

$$\tau_2 = 2\sqrt{LC}\cos^{-1}\left[\frac{E/k - E}{-\left(E - \frac{v_o}{2}\right)}\right] \qquad \text{(II-6)}$$

Since,

$$\frac{E/k - E}{-\left(E - \frac{v_o}{2}\right)} < 0 \text{ , then } \frac{1}{2\sqrt{LC}}\tau_2 > \pi/2 \qquad \text{(II-7)}$$

When t reaches this value, the current in the inductor is:

$$i_\Delta = 2\left(E - \frac{v_0}{2}\right)\sqrt{\frac{C}{L}}\sin\left\{\cos^{-1}\left[\frac{E/k - E}{-\left(E - \frac{v_0}{2}\right)}\right]\right\} \qquad \text{(II-8)}$$

$$= 2\left(E - \frac{v_0}{2}\right)\sqrt{\frac{C}{L}}\sqrt{1 - \left[\frac{E/k - E}{-\left(E - \frac{v_0}{2}\right)}\right]^2}$$

The currents in the circuit immediately before the capacitor C reaches its maximum voltage of 2E/K are shown in Figure II-4. The currents immediately after are shown in Figure II-5. The current i_2 is now forced around the SCR 1-D1 loop by the inductor L; the current i_3 flows in order to maintain the NI relationship in the output transformer. The voltage across the fraction of the transformer between D1 and the battery is E; therefore the voltage across that part of the transformer winding between D1 and SCR 1 is given by E. Assuming the diodes and SCR's have no internal drops, this voltage is the only one opposing the change of current in L, and this current thus decreases at a rate of

$$\frac{E}{L}\ \frac{(1-K)}{(K)}\ \text{amp/sec.} \qquad \text{(II-9)}$$

The time required for the current to die to zero is thus given by $\frac{I}{-di/dt} =$

$$\frac{Lk}{E(1-k}\ \left(E - \frac{v_0}{2}\right)\sqrt{\frac{C}{L}}\sqrt{1 - \left[\frac{E/k - E}{-\left(E - \frac{v_0}{2}\right)}\right]^2} \equiv \tau_3 \text{ seconds} \qquad \text{(II-10)}$$

and the current i_2 during this interval is given by:

$$i_2 = 2\left(E - \frac{v_0}{2}\right)\sqrt{\frac{C}{L}}\sqrt{1 - \left[\frac{E/k - E}{-\left(E - \frac{v_0}{2}\right)}\right]^2}\left\{1 - \frac{t - \tau_2}{\tau_3}\right\} \qquad \text{(II-11)}$$

where t = o is the time of initial gating on of SCR 1. (This is just a linear decay in τ_3 seconds from the initial value of the current as given by equation II-8).

The current i_3 which must flow to maintain the NI relationships in the output transformer is given by (II-12)

$$i_3 = i_2 \left(\frac{1-K}{K} \right)$$

and the integral

$$\int_{\tau_2}^{\tau_3} E i_3 \, dt = \frac{E(1-K)}{K} \int_{\tau_2}^{\tau_3} i_2 \, dt \qquad \text{(II-13)}$$

represents the excess energy stored in the inductor being returned to the battery. These currents are also shown in the waveform drawing of Figure II-10.

From these equations can be seen the reasons for having $K < 1$; if $K = 1$, (i.e., the diodes D_1 and D_2 were connected to the ends of the transformer where SCR 1 and SCR 2 respectively are) the current i_2 would continue to circulate in the L, SCR 1, D_1 loop indefinitely. (Of course, the resistance in these elements would tend to damp the currents, but all the excess energy stored in the inductance L would be dissipated in the circuit elements instead of being returned to the battery.)

The smaller K is made, the faster the energy stored in the choke is returned to the battery. However, as K is made smaller, the higher the voltage across

the transformer must rise in order for the reactive diodes to become effective, and the higher the internal impedance of the inverter during reactive current periods becomes. A practical minimum value for K is 0.8.

At the end of this period of returning energy to the battery (during which the capacitor voltage has been maintained at 2E/K volts,) the commutating capacitor discharges into the load until its voltage drops to 2E volts.

If the load current at this time is I_1, then the capacitor current is $\frac{I_1}{2}$ (the transformer has a 1:1:1 turns ratio) and its voltage then changes at a rate of

$$\frac{dv}{dt} = i/c = \frac{I_1}{2C} \quad \text{volts/sec} \qquad \text{(II-14)}$$

The change in voltage is $\frac{2E}{k} - 2E = 2E\left(\frac{1}{k} - 1\right)$ volts; thus the time required is

$$\Delta t = \frac{\Delta v}{dv/dt} = \frac{2E\left(\frac{1}{k} - 1\right)}{I_1/2C} = \frac{4CE\left(\frac{1}{k} - 1\right)}{I_1} \quad \text{seconds} \qquad \text{(II-15)}$$

When this discharge has been completed, the load current is again carried by SCR 1. For a resistive load, nothing further happens until SCR 2 is gated on.

When SCR 2 is turned on, then the cycle as started with Figure II-2 is repeated, only now SCR 1 must be turned off and the initial voltage on the capacitor is -2E. Equations II-1 through II-15 can thus be used to describe the action that occurs in the steady state, if v_0 is set equal to -2E. A complete cycle of operation is shown in Figure II-10. This diagram is for the case of a pure resistive load with the output frequency of the inverter low enough so that it can be assumed that the reflected load current is constant (and zero) during

the switching interval.

The time scale on this diagram is not constant; the switching intervals are expanded to show in detail the waveforms at commutation while the later period of operation is shown more to scale. Values of current and voltage are indicated and are obtained from formulas developed previously. At higher frequencies where the expanded portion of the waveform (the switching interval) becomes an increasing fraction of the total cycle, exact analysis becomes more difficult, however, for most regions of interest, the current due to switching and the load may be superimposed, because the SCR forward drop is substantially independent of current.

When load current is non-zero during the commutation period, (as will occur for reactive loads) the circuit operation becomes more involved but can be analyzed as follows: Since it has been assumed that the filter passes only fundamental current, the load current can be written

$$i_L = A \sin(\omega_0 t - \theta_z) \qquad \text{II-16}$$

where W_o is the fundamental (output) angular frequency of the inverter (and filter) and θ_z is the angle of the combined load and filter impedance as seen by the power stage. Under the assumption that the commutation time is small compared to the period of the fundamental frequency, the load current during the commutation interval is approximately constant. This value may be anywhere between -A and+A depending on the phase angle of the load impedance as seen by the inverter output transformer. Furthermore, with the operating

frequency much less than the natural resonant frequency of L and C (which will be on the order of 20 KC), the voltage developed across the inductor L by the changing current at the fundamental frequency is negligible. Under these assumptions the voltages and currents during the commutation period will be examined.

Immediately prior to the turning on of SCR 2, the voltages and currents in the circuit are as shown in Figure II-6. (For this discussion, an inductive load has been assumed, so at the time of commutation of SCR 1, there is a current flowing in it from the load). SCR 1 (about to be commutated) is carrying i_4 the (1:1) transformed load current i_L.

$$\text{At } t = \frac{\pi}{\omega_0} \qquad i_4 = i_L = A\sin(\pi - \theta_z) = A\sin\theta_z \equiv I_0 \tag{II-17}$$

At the instant after SCR 2 is turned on, the voltages and currents are as shown in Figure II-7.

Since the filter maintains the load current constant at I_o at the time of switching, the transformer, in order to maintain the relation $\Sigma NI = 0$, must carry a primary current of I_o as shown. Since the current must also be maintained in the commutating choke, the current path shown for i_5 is the only one possible. (Any current in the now unused half of the primary which would be in the proper direction to maintain the transformer NI relationship would have to flow in the reverse direction through SCR 2; this is not allowed.) SCR 1 will be reverse biased until the capacitor voltage reaches zero. If this were

the only current flowing, the capacitor would reach zero volts at

$$\Delta t = \frac{C\Delta E}{I} = \frac{2EC}{I_o} \qquad \text{(II-18)}$$

However, there will also be a current flow into the capacitor as SCR 2 attempts to charge it up to 2E through the transformer. The current directions for this action are shown in Figure II-8.

An exact solution for the available turn-off-time (under the assumption that the load current does not change during the commutation interval) can be obtained as follows. Figure II-9A represents the circuit as SCR 1 is turned on. Here I_o is the reflected load current (assumed constant, as shown) and i is the capacitor charging current.

Under the assumption that the transformer is ideal and that the load current remains constant during commutation, the equivalent circuit of Figure II-9A becomes as shown in Figure II-9B.

The equations for this circuit are

$$\frac{v_c}{2} = \frac{v_o}{2} + \frac{1}{4C}\int_0^t (2I_o + i)\,dt \qquad L\frac{di}{dt} = E - \frac{v_c}{2} \qquad \text{(II-19)}$$

Eliminating VC/2, there results

$$E - L\frac{di}{dt} = \frac{v_o}{2} + \frac{1}{4C}\int_0^t (2I_o + i)\,dt \qquad \text{(II-20)}$$

Differentiating this and rearranging terms yields:

$$\frac{d^2i}{dt^2} + \frac{i}{4LC} = \frac{-2I_o}{4LC} \qquad \text{(II-21)}$$

Subject to the initial conditions:

$$\left.\frac{di}{dt}\right|_{t=0} = \frac{E-\frac{v_0}{2}}{L} \qquad \left. i \right|_{t=0} = 0 \tag{II-22}$$

This has the solution:

$$i = -2I_0 + 2I_0 \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E-\frac{v_0}{2}\right)\sin\frac{t}{2\sqrt{LC}} \tag{II-23}$$

The total current into the capacitor is then $i + 2I_0$ or

$$i_{cap} = 2I_0 \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E-\frac{v_0}{2}\right)\sin\frac{t}{2\sqrt{LC}} \tag{II-24}$$

The voltage on the equivalent capacitor 4C will then rise from $v_0/2$ (where v_0 will actually be a negative number) through 0 towards its final value E/K. However, once the capacitor voltage passes through the zero point, the SCR being commutated (in this case SCR 1) is again forward biased, ending the available turn-off-period. The charge that must be added to the capacitor to accomplish this voltage change is

$$\Delta Q = C\Delta V = 4C\left(0-\frac{v_0}{2}\right) = -2Cv_0 \tag{II-25}$$

but

$$\Delta Q = \int_0^t i_{cap}\,dt = \int_0^t \left[2I_0 \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E-\frac{v_0}{2}\right)\sin\frac{t}{2\sqrt{LC}}\right]dt \tag{II-26}$$

Equating these two values of Δq (and performing the integration) there results

$$4I_0\sqrt{LC}\sin\frac{t}{2\sqrt{LC}} - 4C\left(E-\frac{v_0}{2}\right)\cos\frac{t}{2\sqrt{LC}} = -4CE \tag{II-27}$$

Combining the sines and cosines trigonometrically results in the equation:

$$\sin\left[\frac{t}{2\sqrt{LC}} + \tan^{-1}\frac{C\left(E-\frac{v_0}{2}\right)}{I_0\sqrt{LC}}\right] = \frac{-4CE}{\sqrt{\left[4I_0\sqrt{LC}\right]^2 + \left[4C\left(E-\frac{v_0}{2}\right)\right]^2}} \tag{II-28}$$

which has the solution:

$$t = 2\sqrt{LC}\left[\sin^{-1}\left\{\frac{-CE}{\sqrt{I_o^2 LC + C^2\left(E-\frac{v_o}{2}\right)^2}}\right\} - \tan^{-1}\frac{-C\left(E-\frac{v_o}{2}\right)}{I_o\sqrt{LC}}\right] \qquad \text{(II-29)}$$

For the case of a very large current to commutate, this expression reduces to (using the approximations $\sin^{-1}\theta \cong \theta$, $\tan^{-1}\theta \cong \theta$ for θ very small and assuming that $v_o = -2E$)

$$t = 2\sqrt{LC}\left\{\frac{-CE}{I_o\sqrt{LC}} - \frac{-2CE}{I_o\sqrt{LC}}\right\} = \frac{2CE}{I_o} \qquad \text{(II-30)}$$

which agrees with this limiting case value obtained from other reasoning (equation II-18).

The voltage across the capacitor is then (for an initial voltage of -2E):

$$\frac{v_c}{2} = \frac{v_o}{2} + \frac{1}{4C}\int_0^t i\,dt = E + I_o\sqrt{\frac{L}{C}}\sin\frac{t}{2\sqrt{LC}} - 2E\cos\frac{t}{2\sqrt{LC}} \qquad \text{(II-31)}$$

Clearly, the value of v_c at any time t will vary as I_o varies, so, as a limiting case, the situation where I_o is very large will be investigated. For this case the equation for v_c can be written approximately (using the small angle trigonometric relations $\sin\theta \cong \theta$ and $\cos\theta \cong 1$ for θ very small)

$$v_c = -2E + \frac{I_o t}{2C} \qquad \text{(II-32)}$$

and γ_4, the time at which $v_c = 2E/k$

is given by $\gamma_4 = \frac{4EC}{I_o}\left[1 + 1/k\right]$ (II-33)

When t reaches this value, the load current, which previously went into the capacitor, now flows into the reactive diode. Because the capacitor was

charged up so rapidly, the amount of extra current built up in the commutating inductor is neglibible.

The current trapped in the commutating choke (the sum of the load and capacitor charging currents at the instant when the capacitor voltage reaches E/K, although in this case the capacitor charging current has been taken as negligible compared to the load current) then decreases at the rate of $\frac{E}{L}\frac{(1-k)}{k}$ amps/sec until it reaches zero.

For accurate results, the actual final current in the inductor should be used as the starting point of this linear decay. From equation II-23 and Figure II-9A, it can be seen that the current in the inductor at any time t for which these equations are valid (which is the time from the start of commutation until the reactive diodes start to conduct) is given by

$$i_L = I_0 + i = -I_0 + 2I_0 \cos\frac{t}{2\sqrt{LC}} + 2\sqrt{\frac{C}{L}}\left(E - \frac{V_0}{2}\right)\sin\frac{t}{2\sqrt{LC}} \qquad \text{(II-34)}$$

and the largest value of t for which this is valid is given by the solution of equation II-26 for the case where $\Delta Q = 4C\left[E/k - V_0/2\right]$
The reactive load current continues to flow through diode D_1 however, resulting in a back bias of $\frac{E(1-k)}{k}$ volts on SCR 1 through the action of the transformer windings. This reactive current is in a direction so as to charge the battery, indicating that, in this portion of the cycle, reactive energy stored in the load during a previous cycle is being returned to the d. c. supply. Sometime before the half-cycle is half over, the load current must reverse its

direction, and energy once again flows from the battery to the load via current through SCR 1 and the commutating choke. When the half cycle is over, SCR 2 is turned on and the process repeats, but with the load current reversed and SCR 1 and D1 changing places with SCR 2 and D2. This is shown on the waveform drawing of Figure II-11 which, like the previous one for a resistive load (Figure II-10) has the first portion of the cycle expanded to show the commutation process in detail.

From previous equations (II-18, II-29, II-30) it can be seen that for the parallel inverter there is a maximum load current that can be commutated; exceeding this value will result in inadequate turn-off time.

For this reason, the simple parallel inverter will not operate with a short circuit or under any other condition which would result in an excessive current flow at the time of commutation. Excessive current not due to the load can occur on starting a parallel inverter if the residual flux levels in the output transformer are not considered. For example, figure II-12A shows

(dashed line) a typical hysteresis loop for a toroidal core, and

(solid line) a B-H curve on which it would be desirable to operate,

from the point of view of making maximum use of the core material. However, because the initial flux level in the transformer could be anywhere between $-B_r$ and $+B_r$ where B_r is the residual flux resulting from the maximum flux level at which the transformer is operated, the first half cycle of applied voltage could easily result in saturating the core. Should the resulting

excessive magnetizing current exceed the maximum commutatible load current, the circuit would malfunction. Also, because toroidal transformers have a very high ratio of B_r to B_{max}, and because of their high permeability tend to drift towards one end of the hysteresis loop under any slight unbalance in the drive, even in a core designed for operation at a low flux density it is possible to end up at a flux level very near to the B_{max} of the core material. This is shown in Figure II-12B, where the dashed line again represents the B-H characteristic of the material and the solid line the desired (and expected) hysteresis loop. The dotted line indicates the loop that would be obtained in the steady state with a slight unbalance in the drive to the transformer, as could occur due to differences in the voltage drops across the switching elements. If an inverter were shut off while operating in this mode, and the next time it was started, the first cycle was of such a polarity so as to further increase the magnitude of this flux, the core would be driven far into saturation and the resulting excessive magnetizing current would cause failure. Thus, unless special precautions are taken to eliminate these problems, toroidal (gapless) transformers should not be used for SCR inverter output transformers. For further discussion and one solution to this problem, the reader is referred to the literature.[10] (As long as the transistors can handle the momentary high peak dissipation, inverters using transistors as the switching element will not be harmed by this occurrance.) The SCR's themselves would not be damaged either, but would fail to be commutated, resulting in system failure. When using ordinary transformer cores, the air gap inherent in the construction of these units results in a residual flux of approximately zero. If a

transformer with gap is then so designed that the maximum operating flux density is less than 1/2 of the saturation flux density, then the application of a full half cycle of voltage at the start will not result in saturation. However, it is not a very efficient use of the core materials to operate them at only 1/2 of their maximum flux levels. This starting problem can be overcome by making the first half cycle of only 1/2 the duration as a normal half cycle. Starting under these conditions is shown in the B-H loop of Figure II-12C. Figure II-13A shows the relationship between the output voltage and core flux level for this starting technique. If we assume that $B_r = 0$, this will result in the core being in the proper dynamic hysteresis loop from the start, and the transformer can be designed to operate near the saturation flux level of the core material. Another variation of this half cycle start idea is to use a high frequency starting technique, where the inverter is started out at least twice the normal operating frequency and the frequency gradually lowered to the operating frequency. This results in a B-H loop which "spirals" out to the steady state condition; again avoiding saturation while operating the transformer at near maximum flux levels in steady state operation. The B-H loop for this condition is shown in Figure II-12D; the relationship between the flux and output voltage for this starting mode is shown in Figure II-13B.

During the commutation period, two parameters of the SCR being commutated are of particular importance: the turn-off-time and the dv/dt rating. The turn-off-time has been already discussed. The dv/dt rating is simply the

maximum rate at which the anode voltage of the SCR can be increased without causing the device to switch into its conducting state. This turning on of the SCR due to rapidly rising anode voltage is actually due to the displacement currents in the gate region induced by the internal anode - gate capacitance of the SCR. For the simple parallel circuit, the value of dv/dt is given approximately by $dv/dt = i_c/C$ where i_c is the current into the commutating capacitor, and is given by

$$i_c = I_0 \cos \frac{t}{2\sqrt{LC}} + \sqrt{\frac{C}{L}} \left(E - \frac{v_0}{2}\right) \sin \frac{t}{2\sqrt{LC}} \qquad \text{(II-35)}$$

(This is one-half the current into the equivalent capacitor of Figure II-11)

The dv/dt on the commutated SCR is thus given by

$$\frac{dv}{dt} = \frac{i_{cap}}{C} = \frac{I_0}{C} \cos \frac{t}{2\sqrt{LC}} + \frac{\left(E - \frac{v_0}{2}\right)}{\sqrt{LC}} \sin \frac{t}{2\sqrt{LC}} \qquad \text{(II-36)}$$

for values of t such that the capacitor voltage is less than 2E/K. For other values of t, the values of dv/dt are less severe than this. Besides this source of dv/dt, the shock excitation of various stray circuit inductances and capacitances which occur at commutation may give rise to very high frequency oscillations which yield high dv/dt's. These oscillations can be effectively damped by putting a series RC stub scross the SCR (anode to cathode). This stub will only be effective for the shock induced dv/dt's described; it will have no value in reducing the I/C component of the dv/dt; if this is too large it must be reduced by a major parameter change. (i.e. increasing C). In general, however, SCR's are available which have dv/dt ratings sufficiently high that they are not a limiting factor in the application of the SCR.

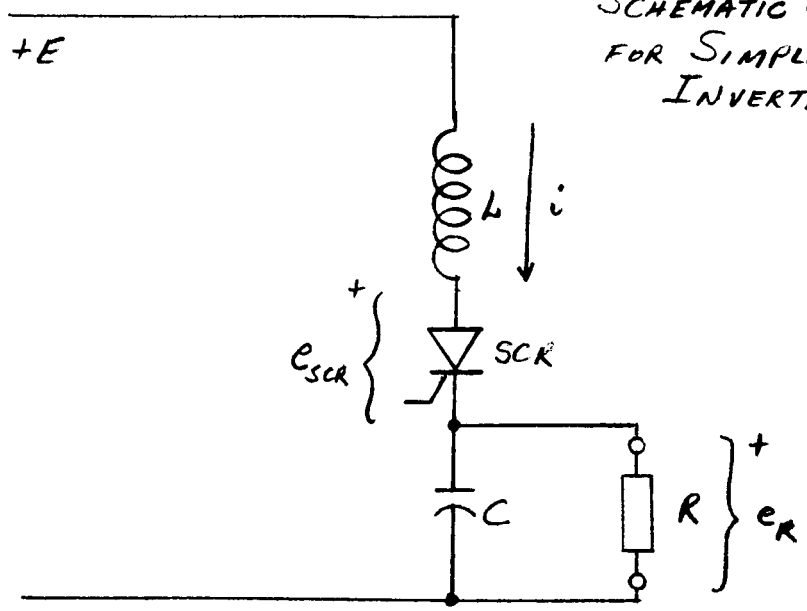
An important rating of the SCR just being turned on at this time which must be observed is its di/dt rating. When an SCR is first turned on, the current it carries is localized in a small area where it was first turned on. Thus, if the initial current allowed by the circuit is too high, the current densities in that portion of the SCR just turned on can cause degrading or destructive local heating. Methods used to minimize this problem are:

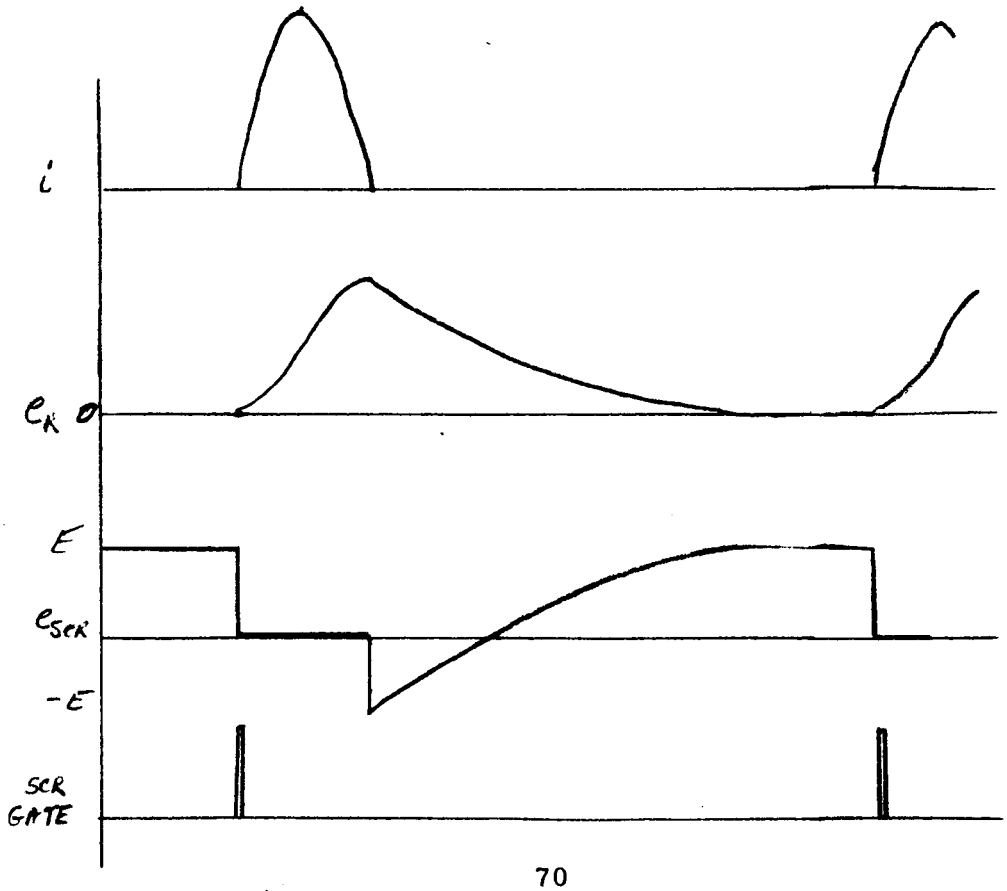
1. To turn on as much of the SCR as possible as soon as possible. This means the use of fast rising gate signals with a peak power capability approaching that of the allowable gate dissipation.

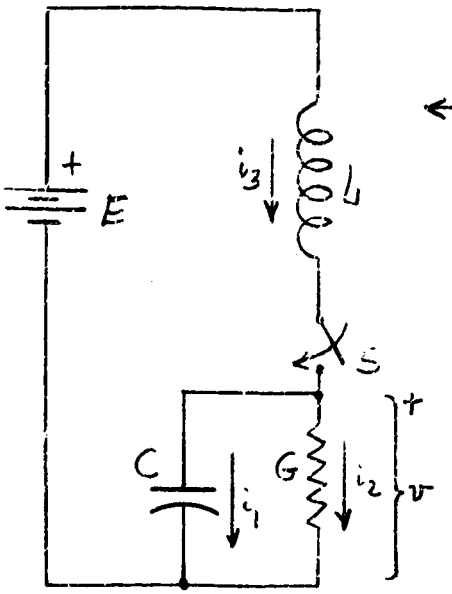
2. To limit the anode current of the SCR during the turn on to as low a value as possible.

Some circuits, for example the series inverter, have small initial currents (see equation 2c, Appendix I) while others, like the parallel inverter, require the SCR to carry a substantial initial current (I_o). In this case, the initial current is limited to a low value for the first few microseconds by putting a small saturating reactor in series with each anode lead.

FIG 1
SCHEMATIC & WAVEFORMS FOR SIMPLE SERIES INVERTER







← FIGURE 1-A
EQUIVALENT CIRCUIT OF FIG. 1 AT TIME OF GATING ON SCR.

FIGURES 1-B THRU 1-F (BELOW)
PLOTS OF $Ge^{Gt/2C}$ (GRAPH ①)
AND $\frac{1}{\omega L} \sin(\omega t + \tan^{-1}\beta)$ (GRAPH ②)
VS t FOR DIFFERENT VALUES OF G
(SEE TEXT FOR DISCUSSION)

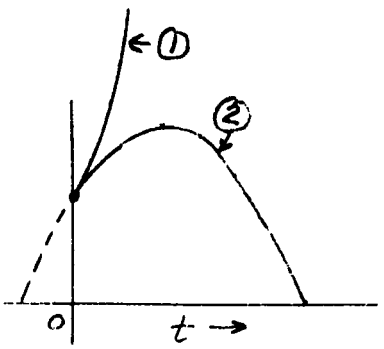


FIG 1-B

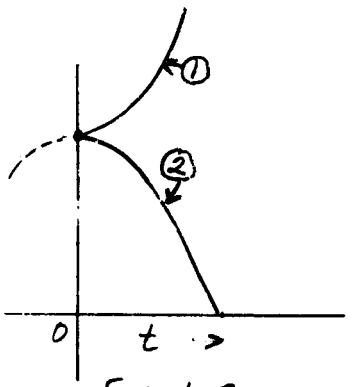


FIG 1-C

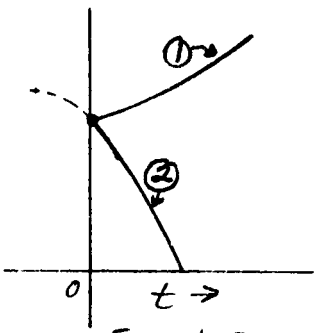


FIG 1-D

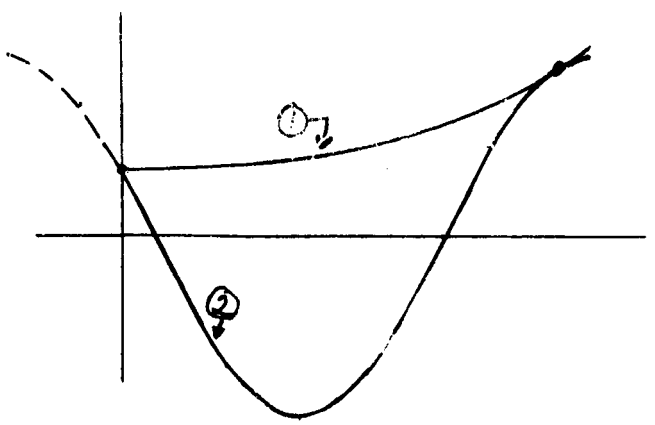


FIG 1-E

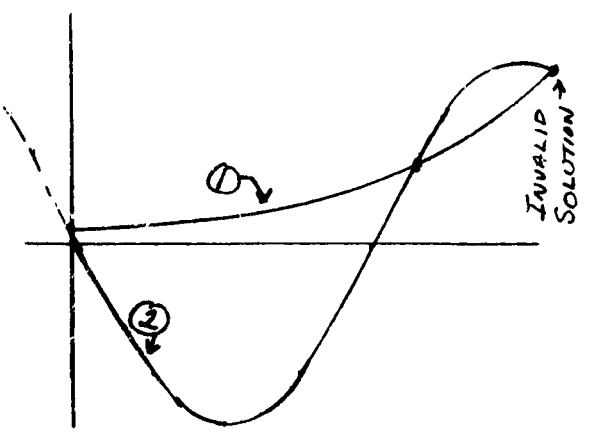


FIG 1-F

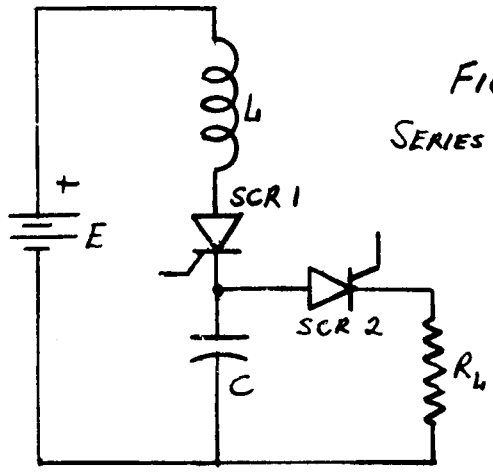
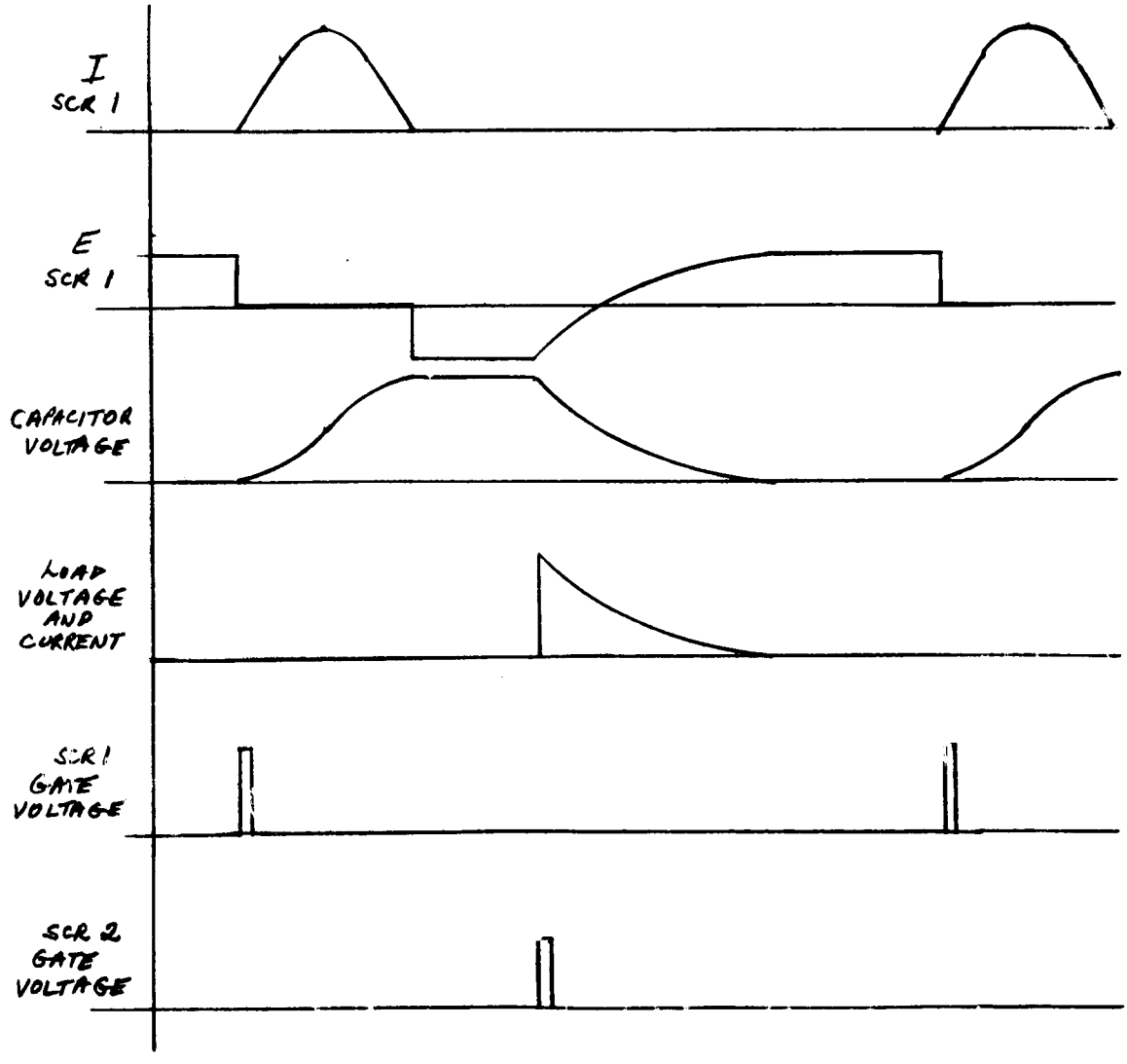


FIGURE 1-G
SERIES INVERTER MODIFIED BY LOAD SWITCH
CIRCUIT AND WAVEFORMS



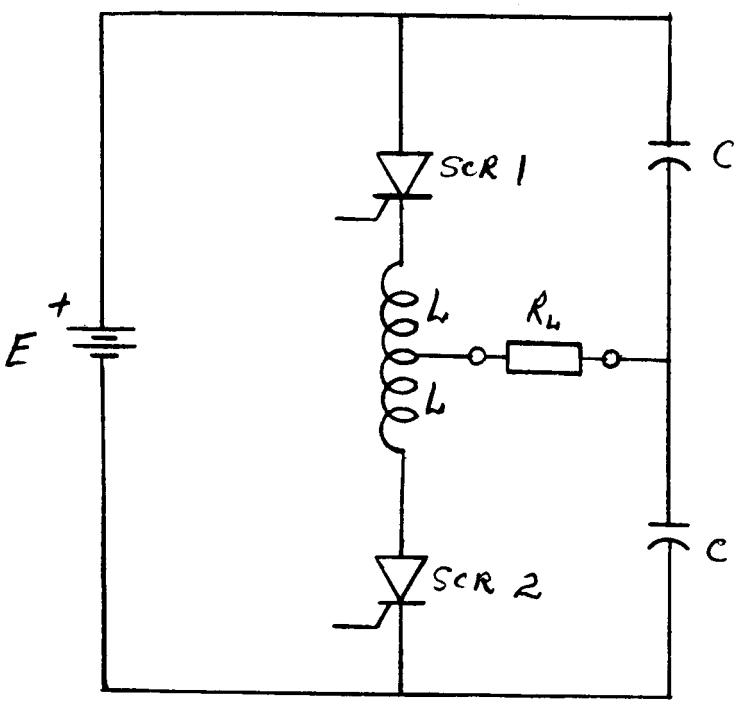


FIG. 2 BIDIRECTIONAL SERIES INVERTER

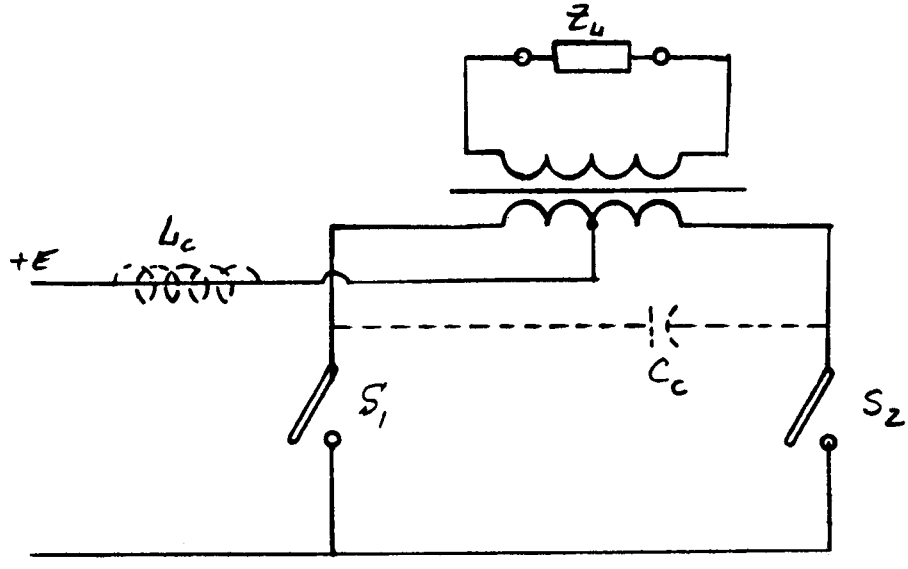
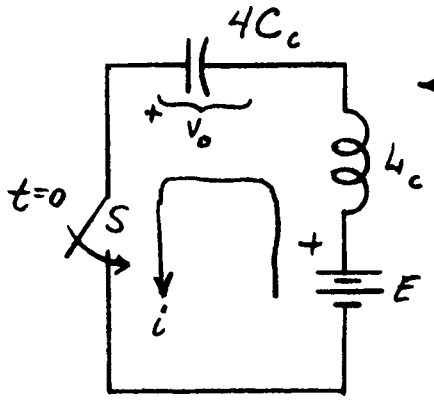
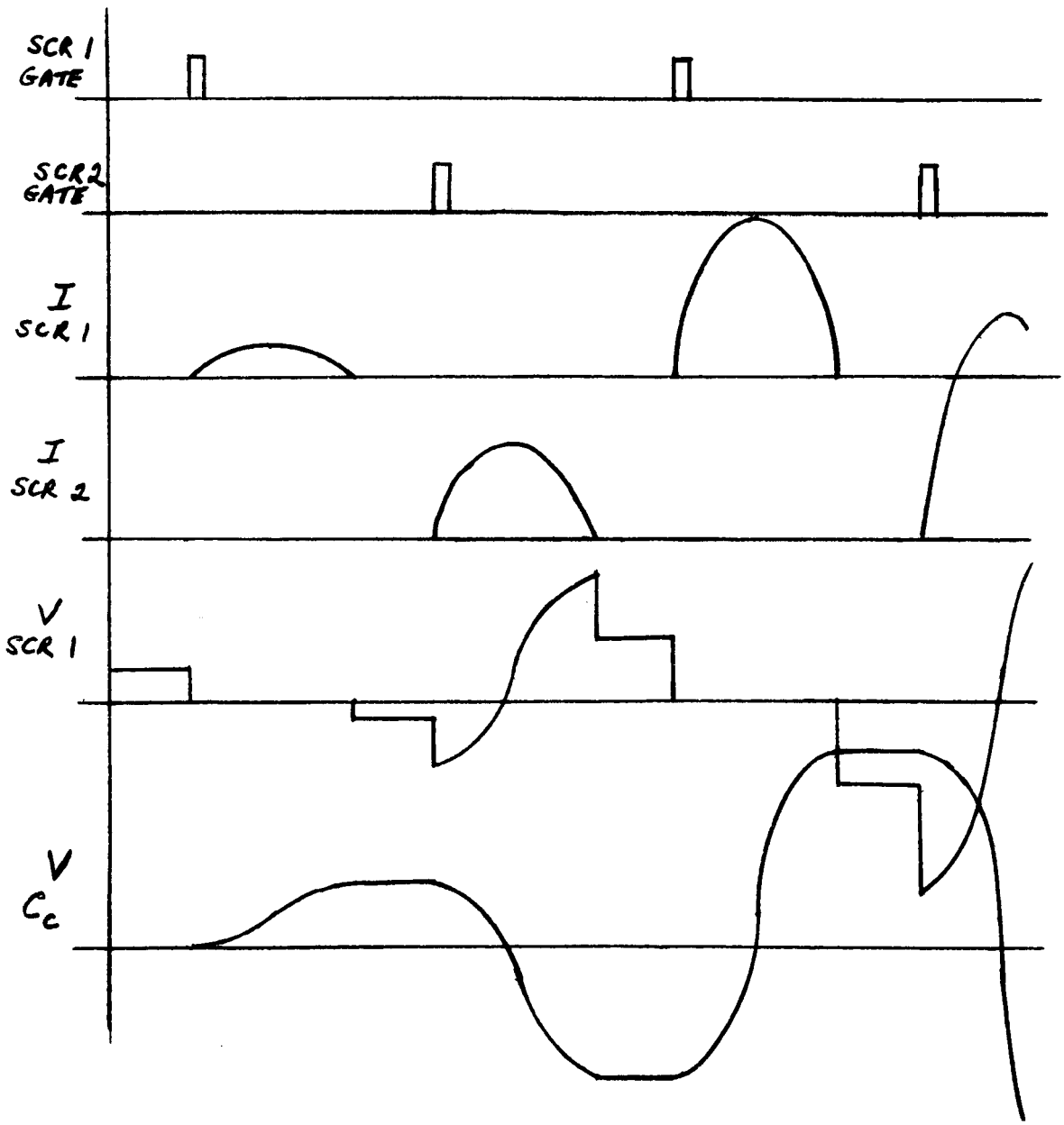


FIG. 3 PARALLEL INVERTER



← FIGURE 3A EQUIVALENT CIRCUIT OF FIG. 3 FOR S_1 BEING CLOSED

FIGURE 3B WAVEFORMS FOR STARTING OF FIG. 3 WITH NO LOAD.



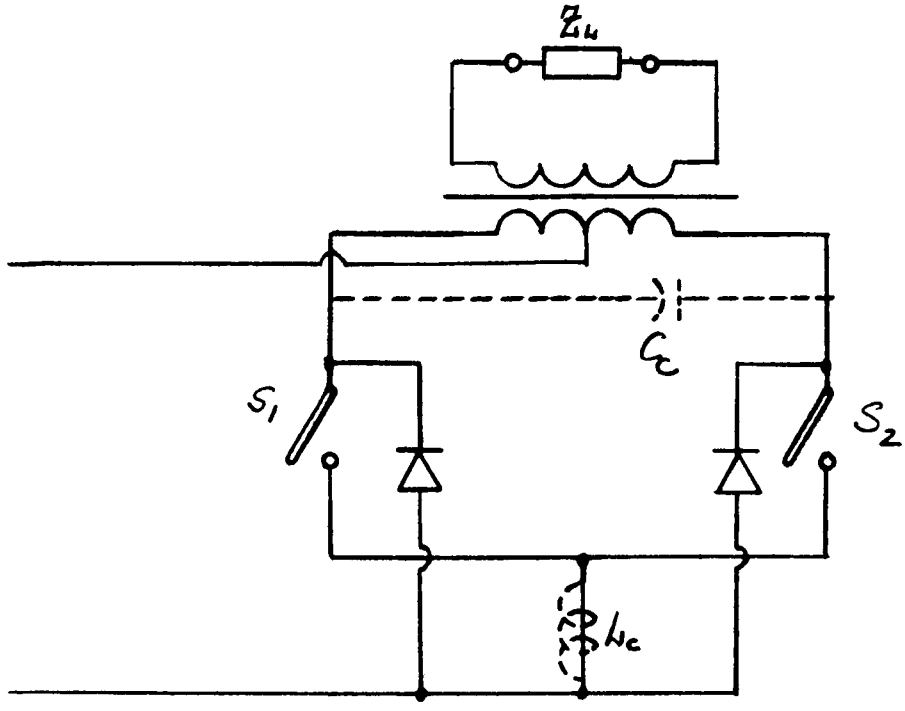


FIG. 4 PARALLEL INVERTER WITH REACTIVE DIODES

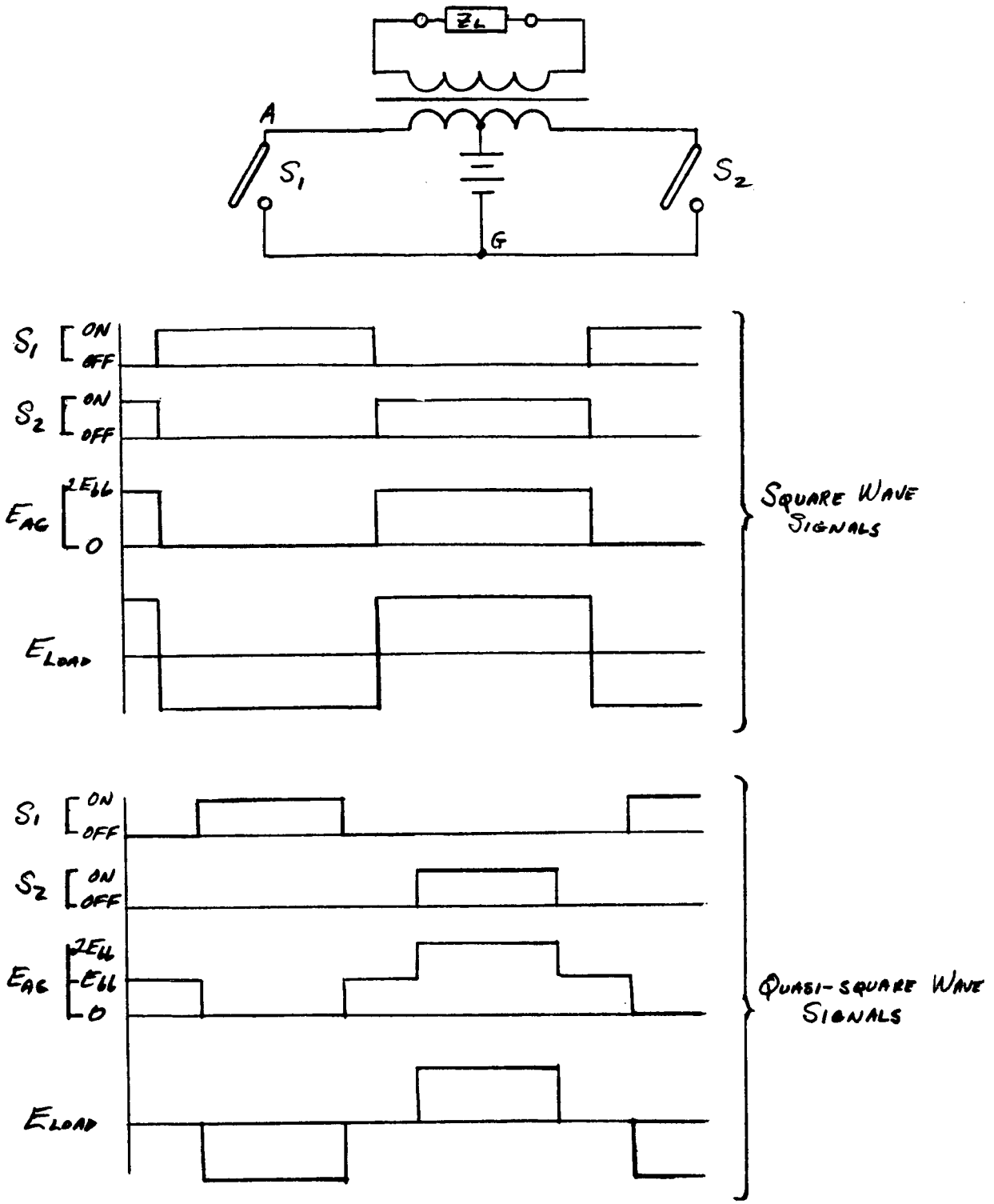


FIG. 5 PARALLEL INVERTER WAVEFORMS

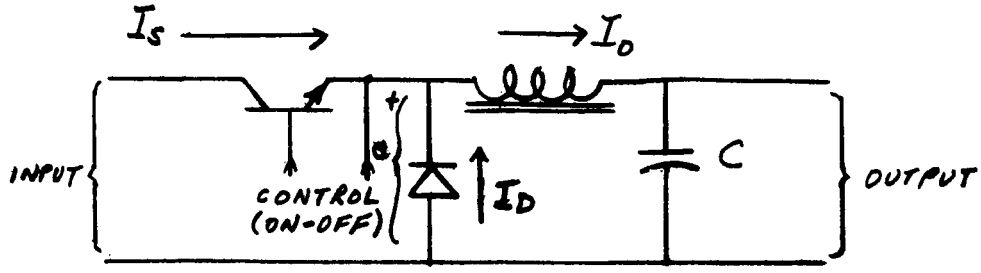


FIGURE 5C SERIES SWITCHING REGULATOR

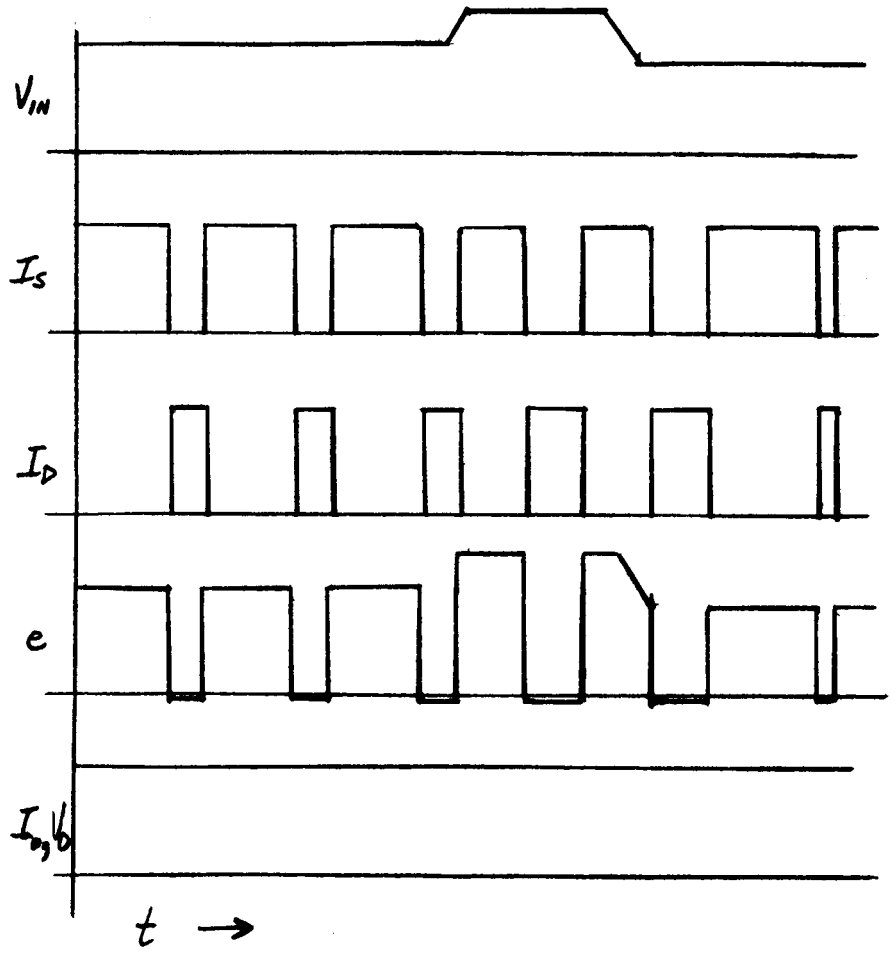


FIG 5D
WAVEFORMS
FOR 5C

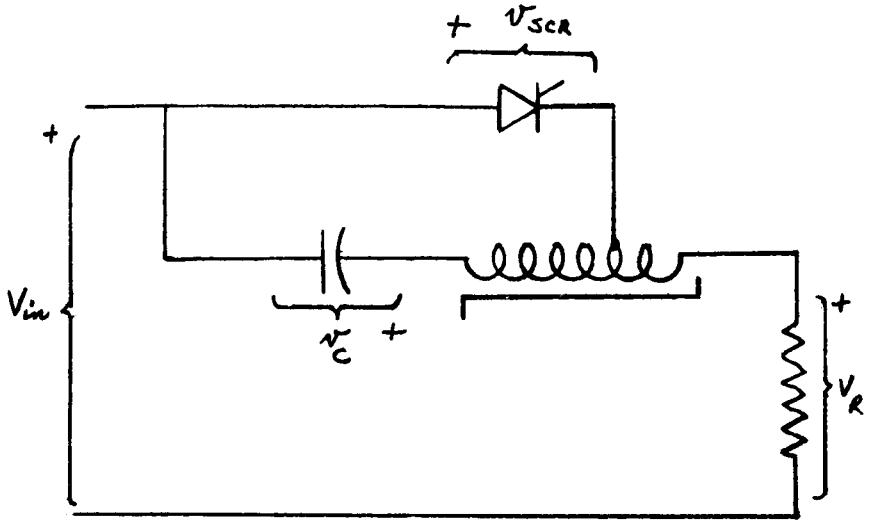


FIG 5E MORGAN CHOPPER CIRCUIT

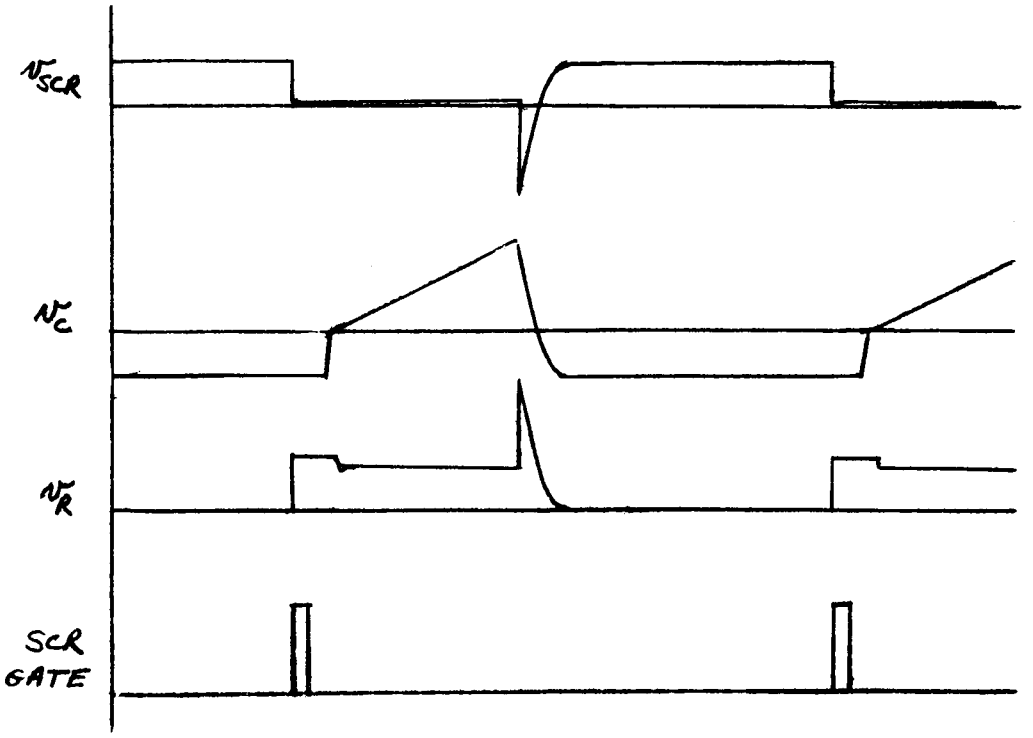


FIG. 5F WAVEFORMS FOR FIG 5E

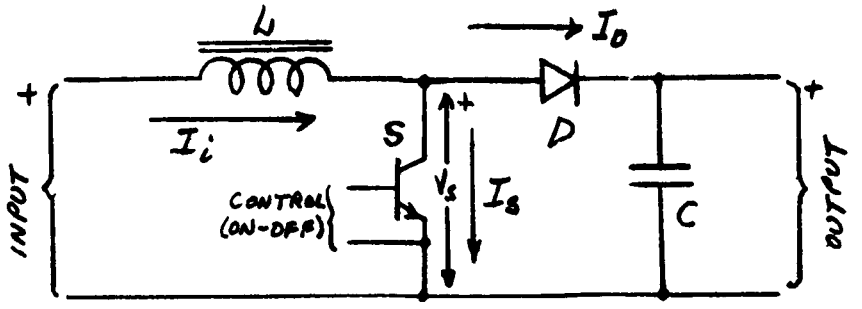


FIG. 5-G BEDFORD STEP-UP CIRCUIT

FIG 5H WAVEFORMS FOR CIRCUIT OF 5-G

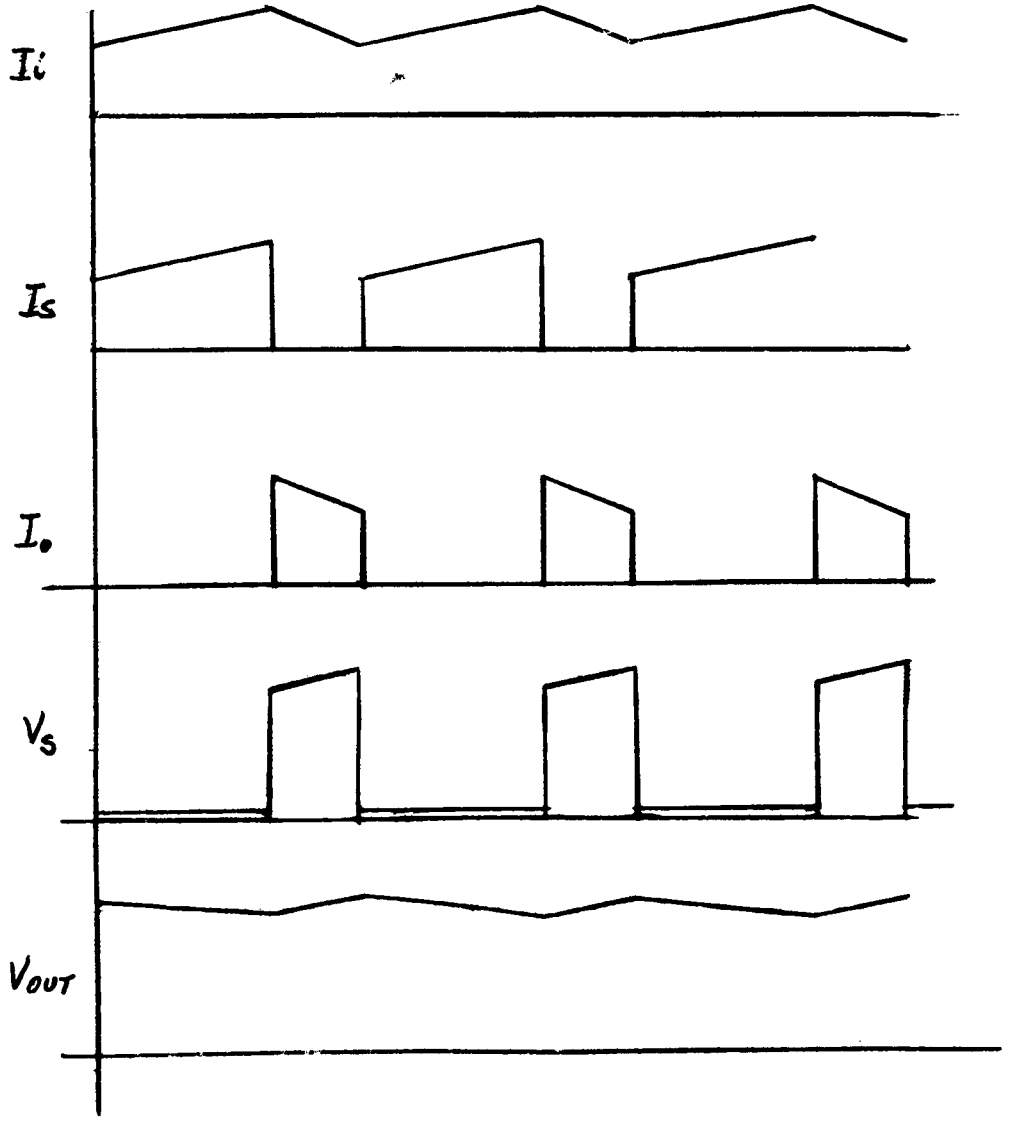
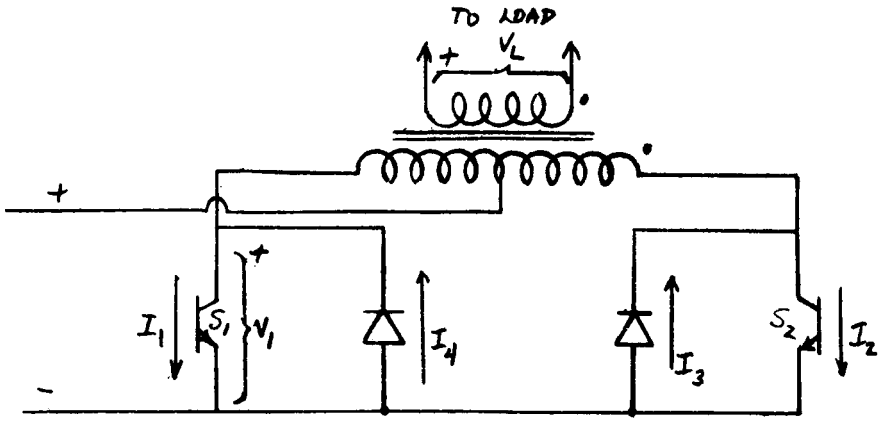
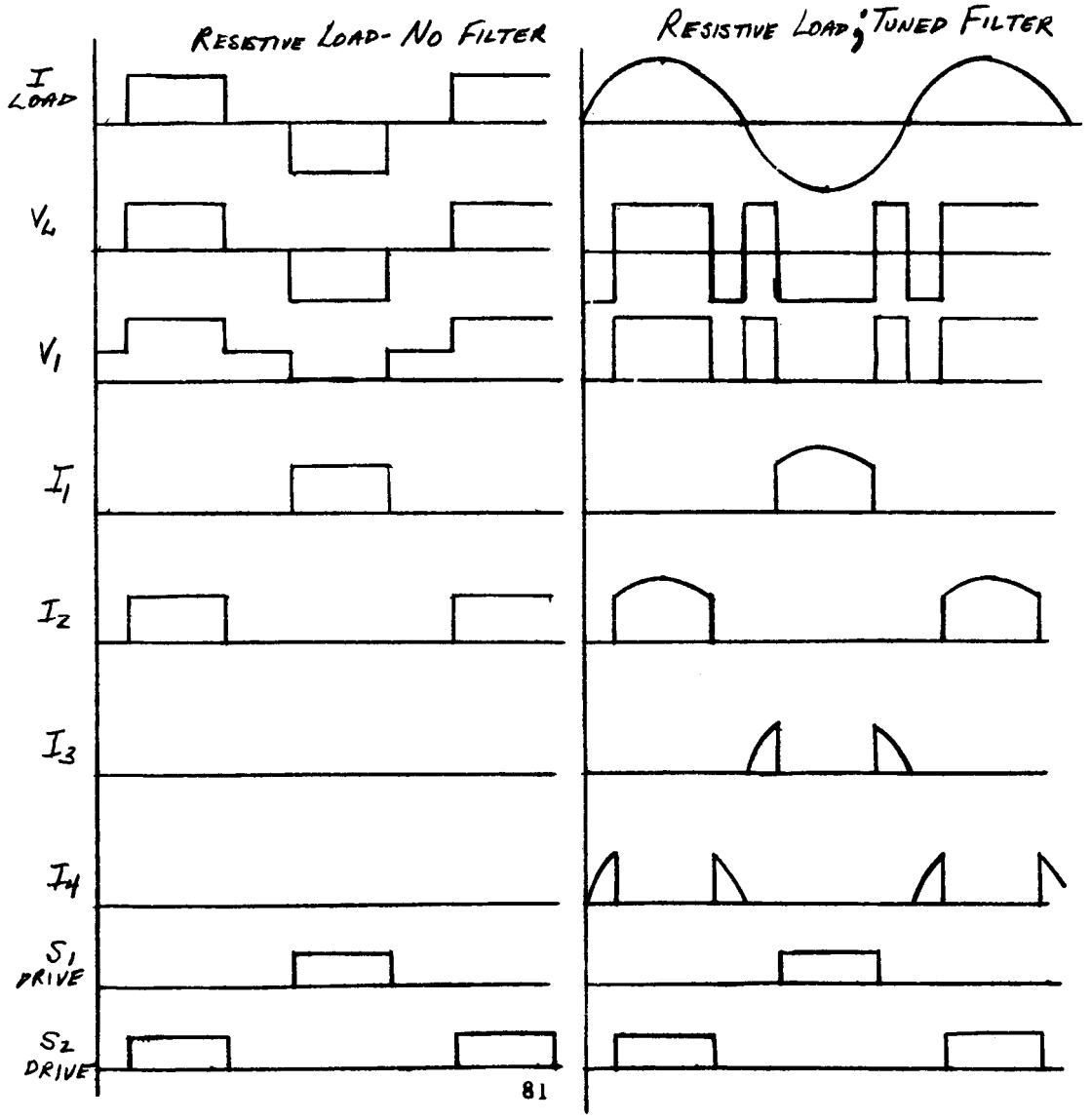


FIG. 5K ILLUSTRATION OF RESULTS OF LACK OF "ZERO CLAMPING"





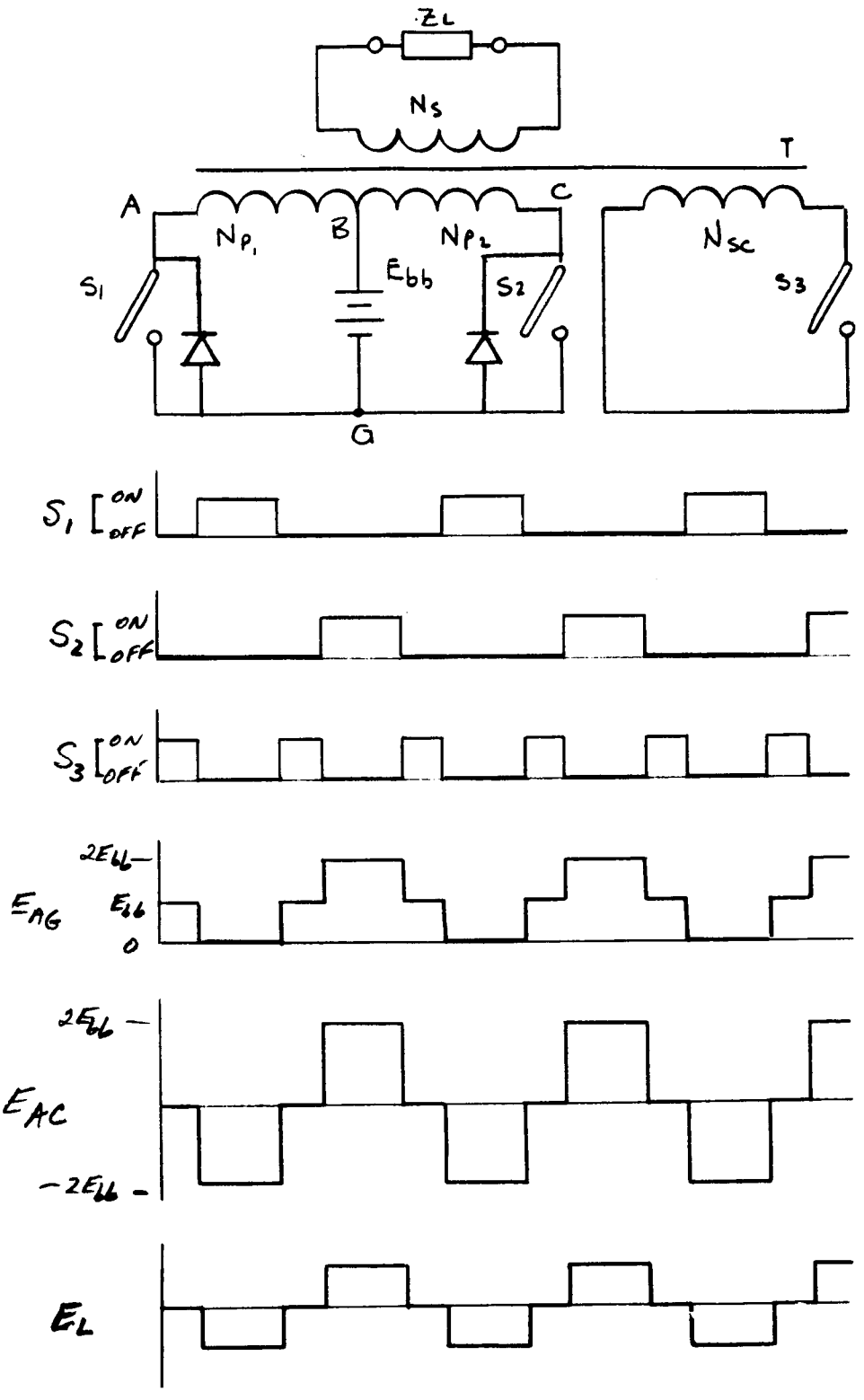


FIG. 6 QUASI-SQUARE WAVE INVERTERS

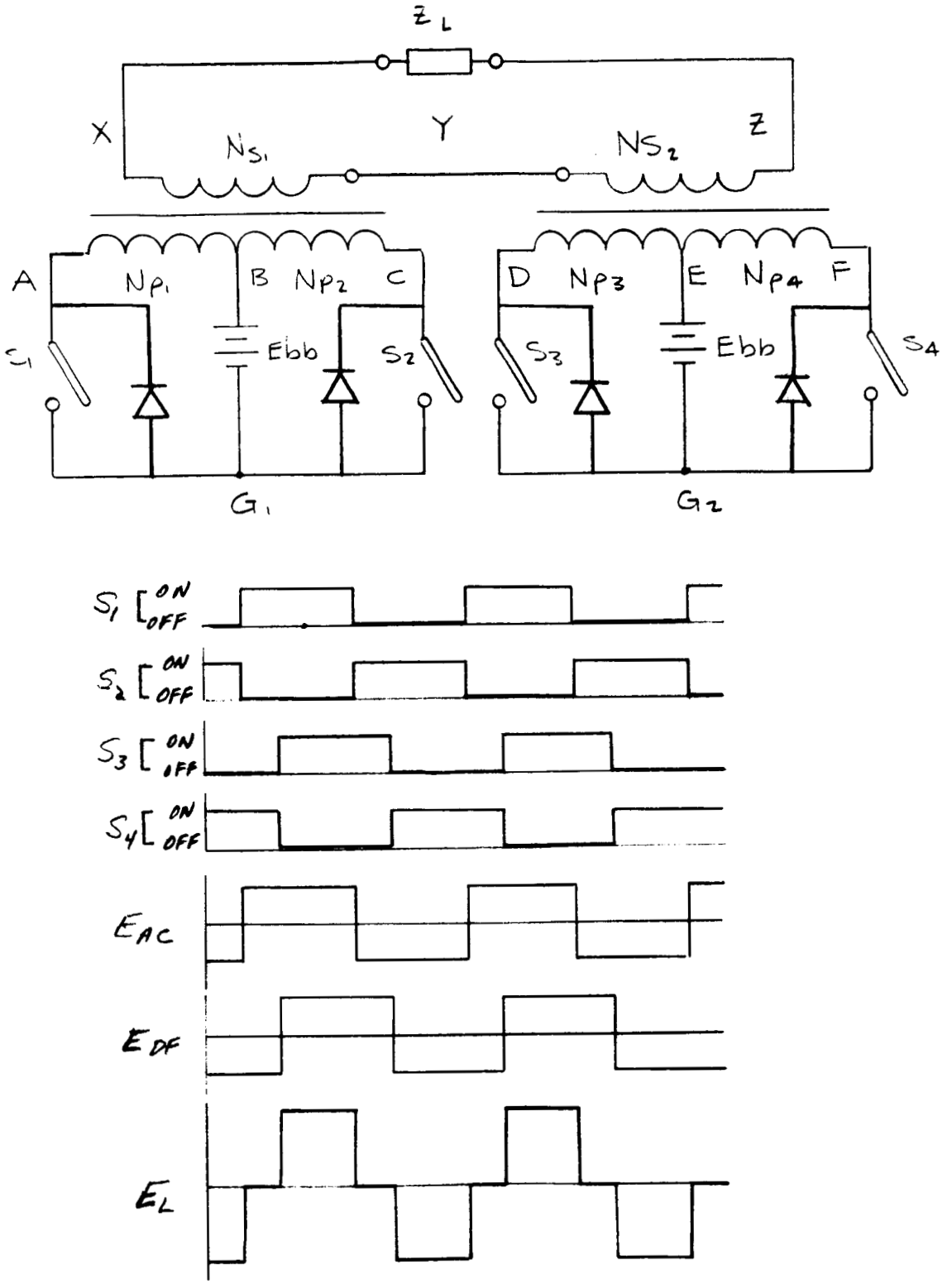


FIG. 7 DOUBLE SQUARE WAVE QUASI-SQUARE INVERTER

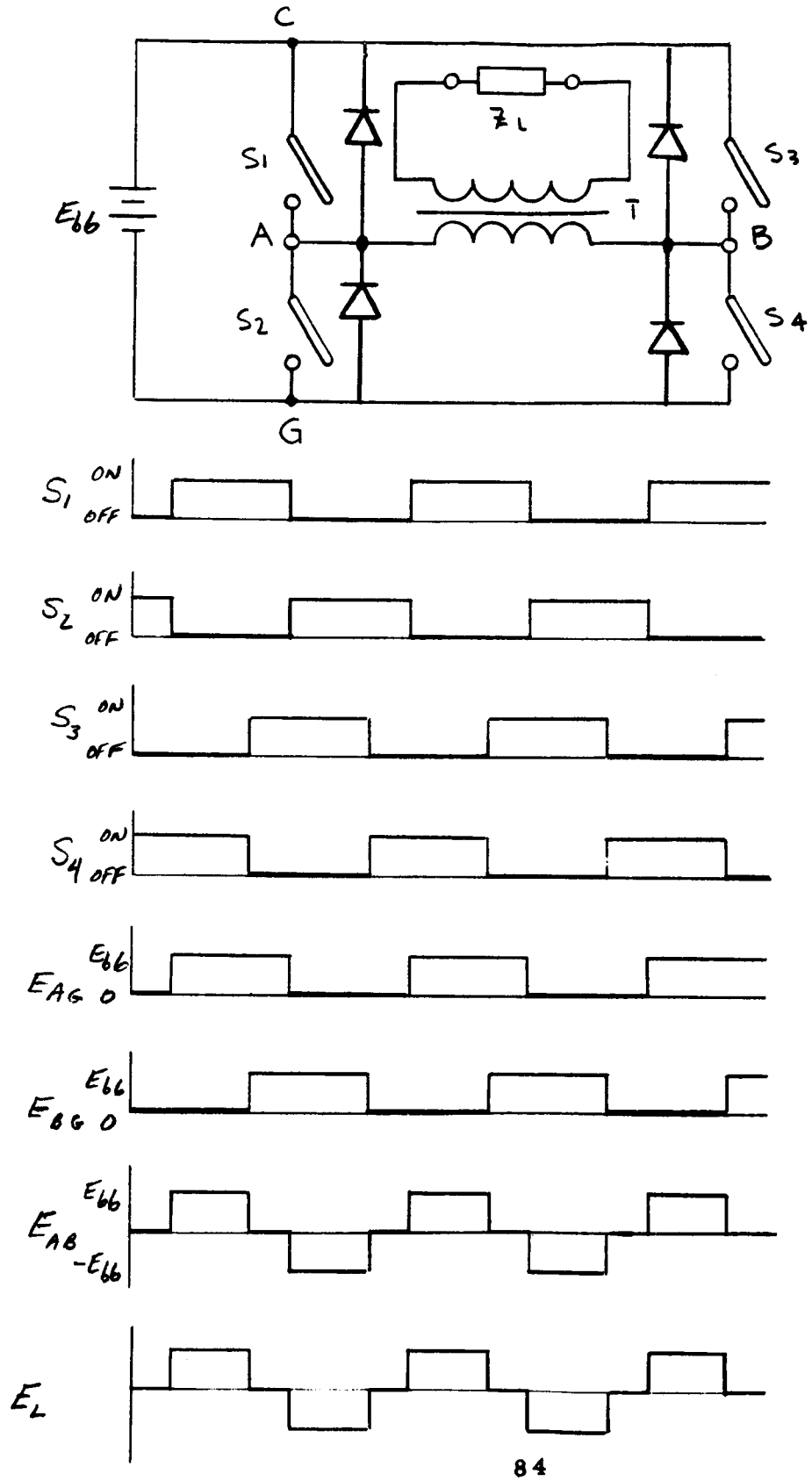


FIG. 8
BRIDGE CIRCUIT

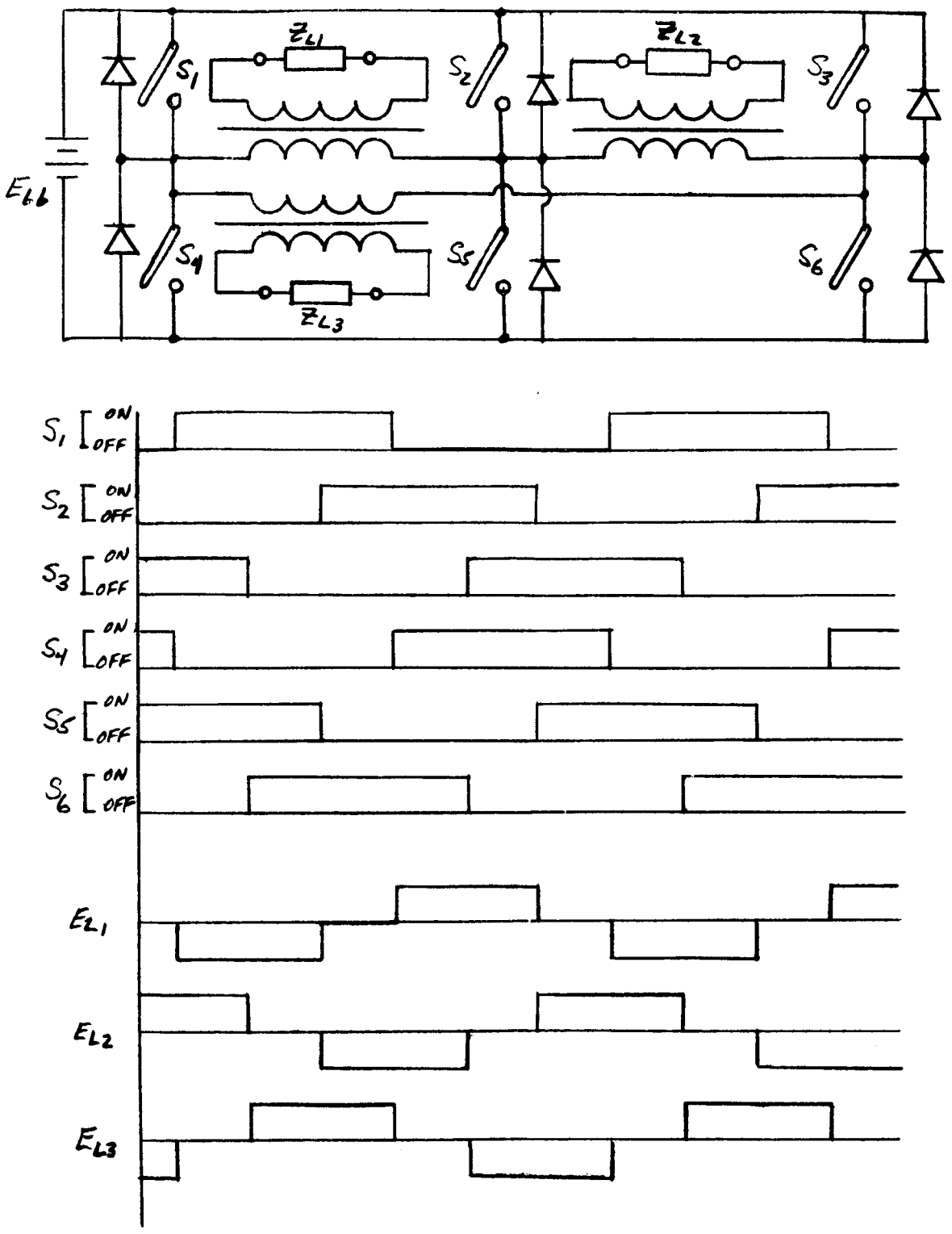


FIG. 9 THREE PHASE BRIDGE INVERTER

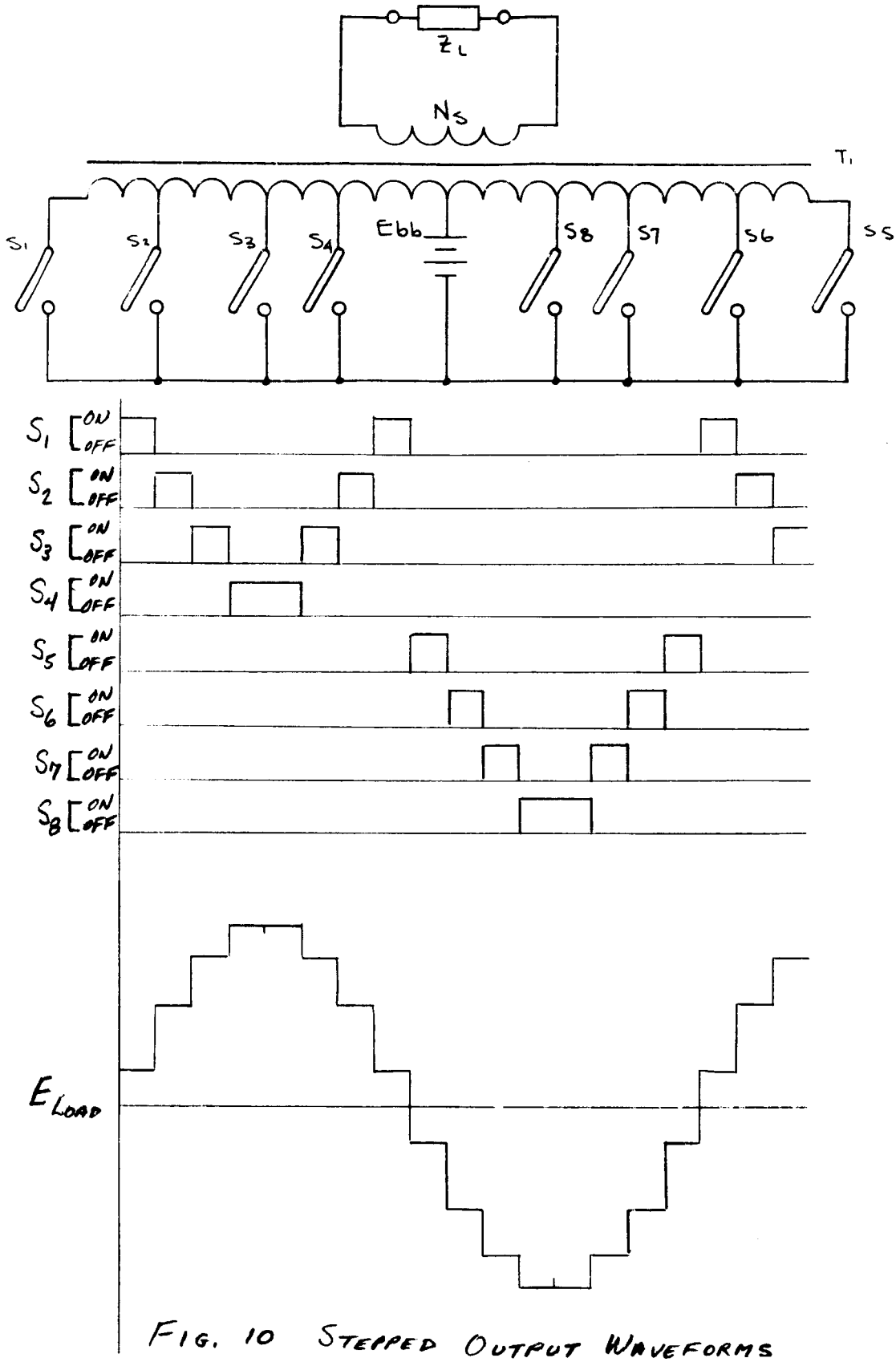


FIG. 10 STEPPED OUTPUT WAVEFORMS

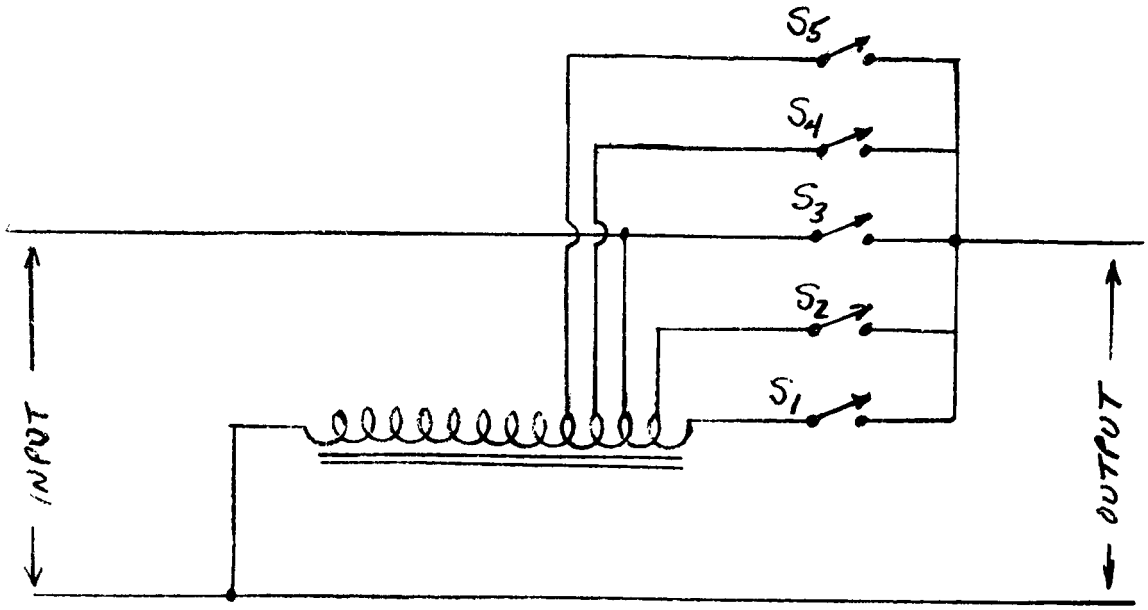


FIG. 10A STATIC TAP CHANGING CIRCUIT

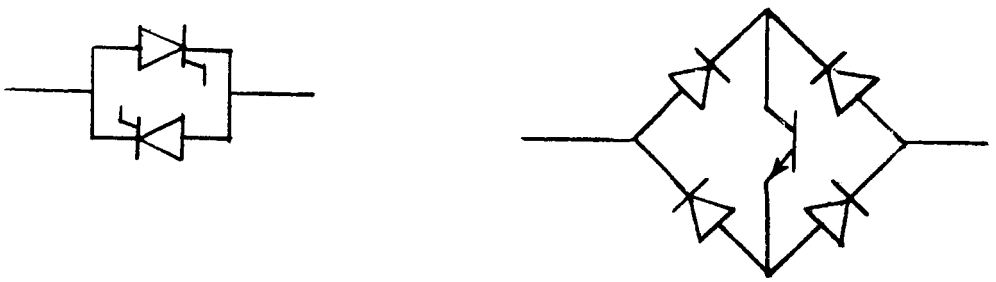


FIG 10B TECHNIQUES FOR REALIZATION OF STATIC SWITCHES FOR A-C USE

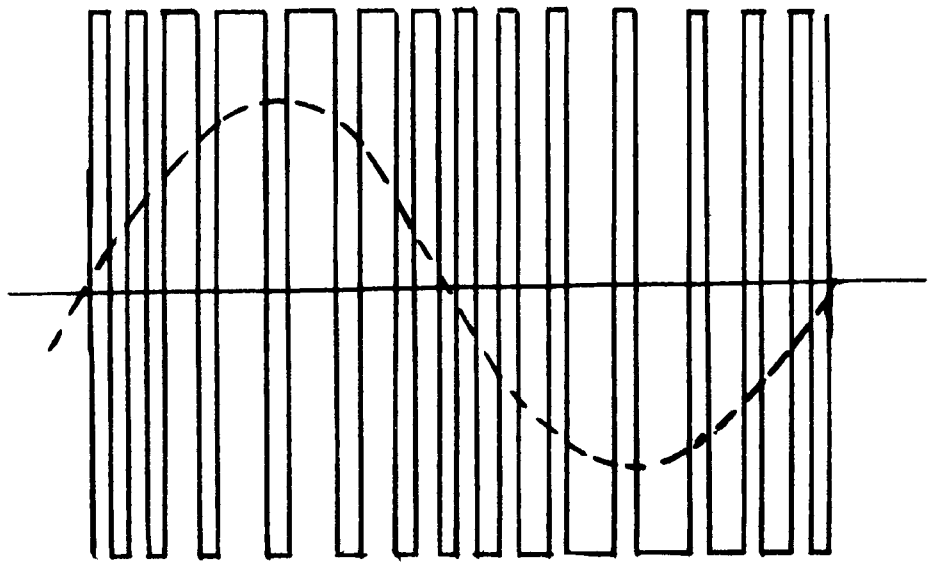
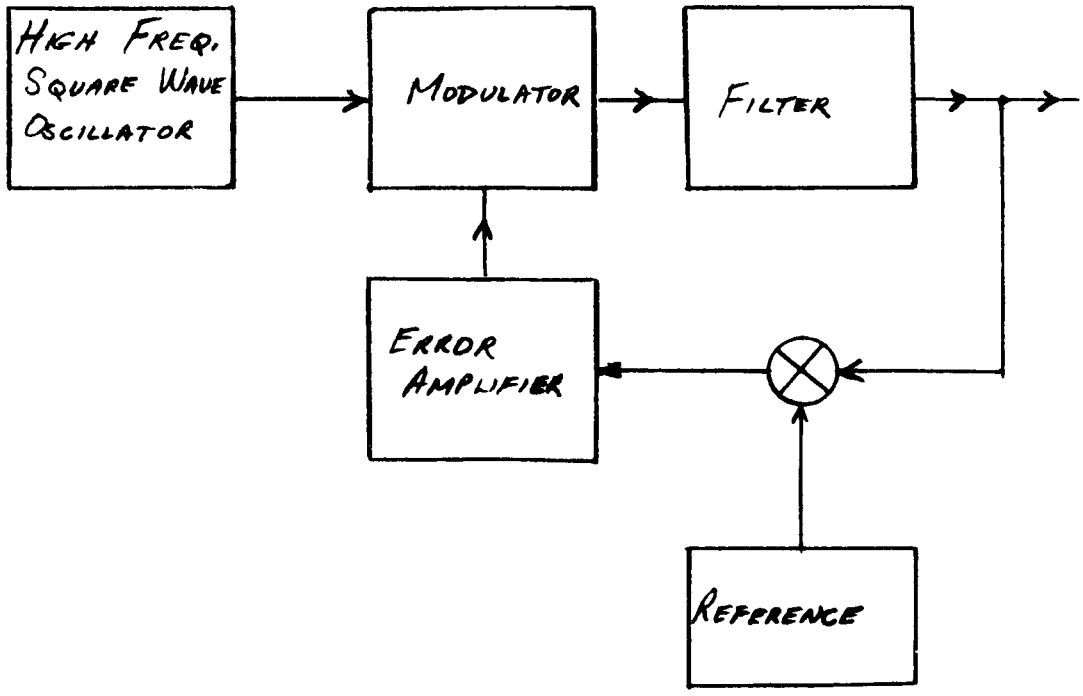


FIG. 11 PULSE WIDTH MODULATION WAVEFORM AND ITS FUNDAMENTAL COMPONENT.

FIG. 12 PULSE WIDTH MODULATION INVERTER - BLOCK DIAGRAM (CYCLO-CONVERTER)



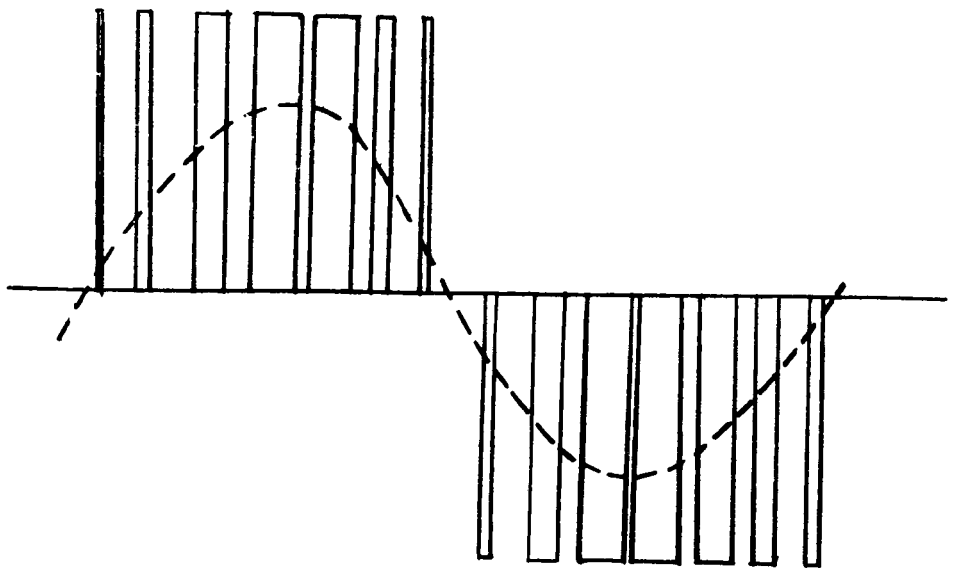


FIG. 13 MODIFIED PULSE WIDTH MODULATION WAVEFORM WITH REDUCED HARMONIC CONTENT, ALONG WITH ITS FUNDAMENTAL COMPONENT.

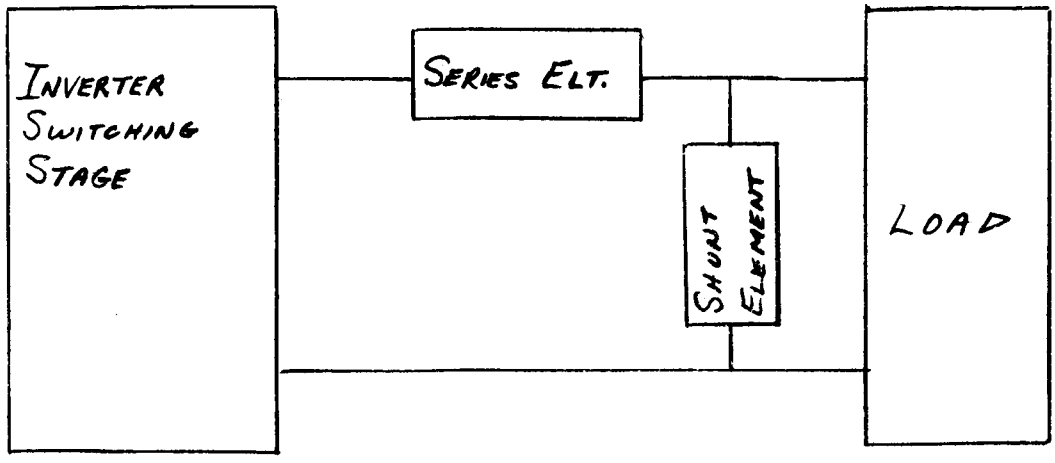


FIG. 14 PASSIVE BANDPASS FILTER
BLOCK DIAGRAM

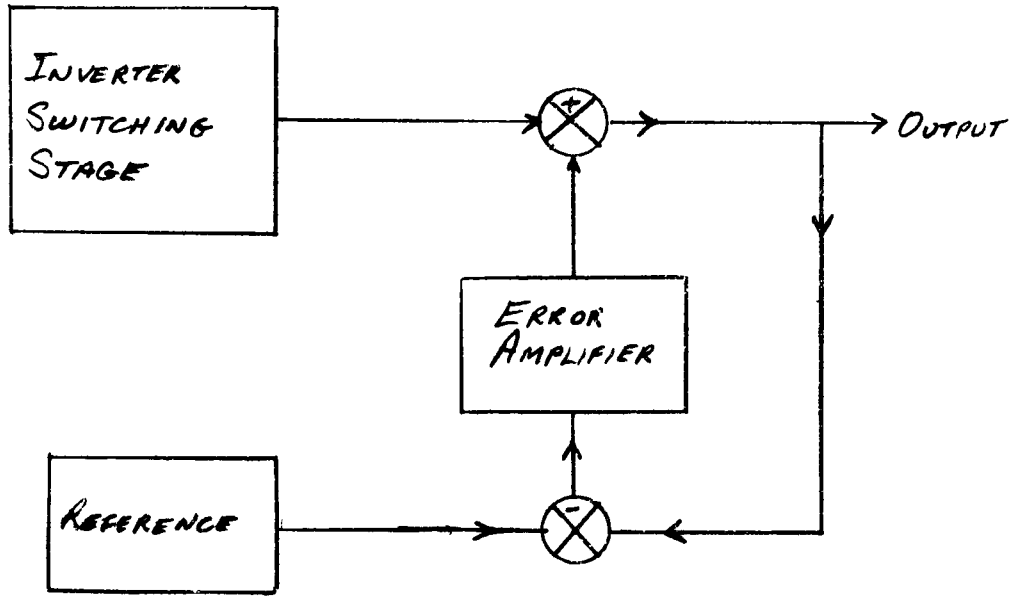


FIG. 15 ACTIVE FILTER
BLOCK DIAGRAM

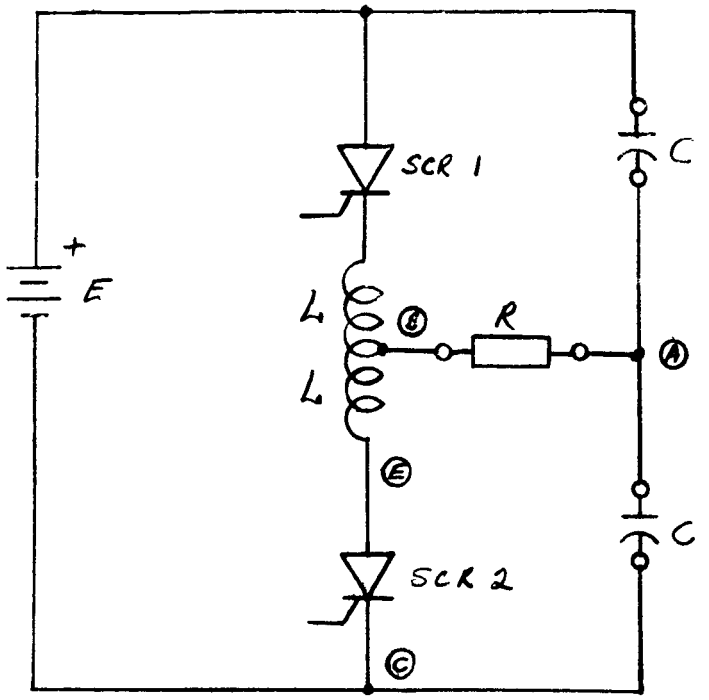


FIG. I-1

BIDIRECTIONAL SERIES INVERTER

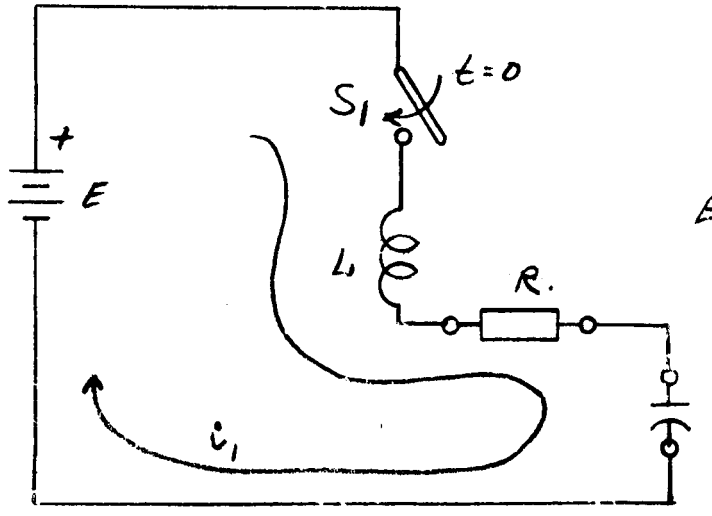


FIG. I-2

EQUIVALENT CKT. OF I-1

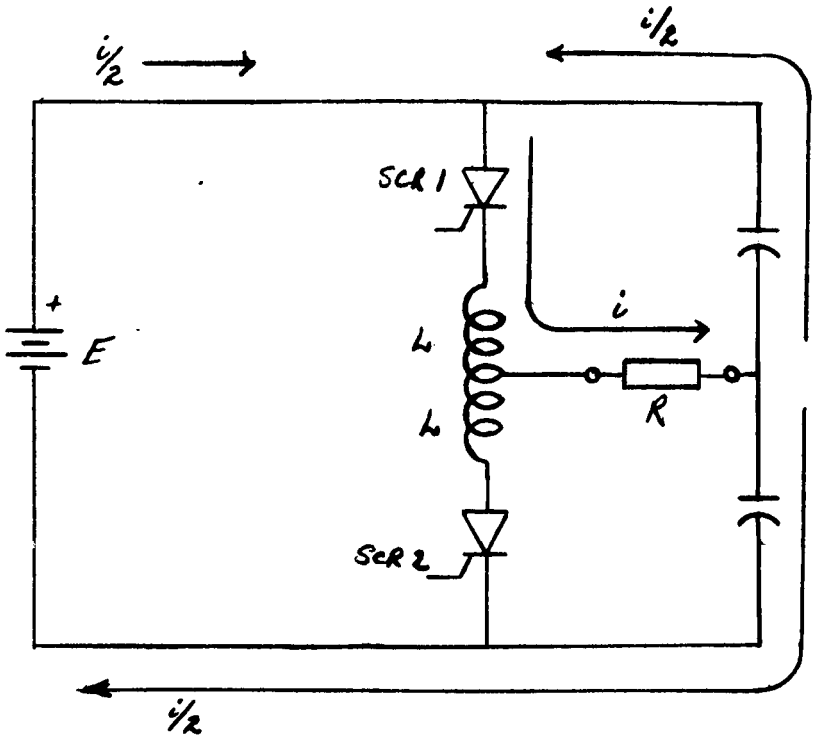


FIG. I-3

SCR 1
CURRENT PATHS

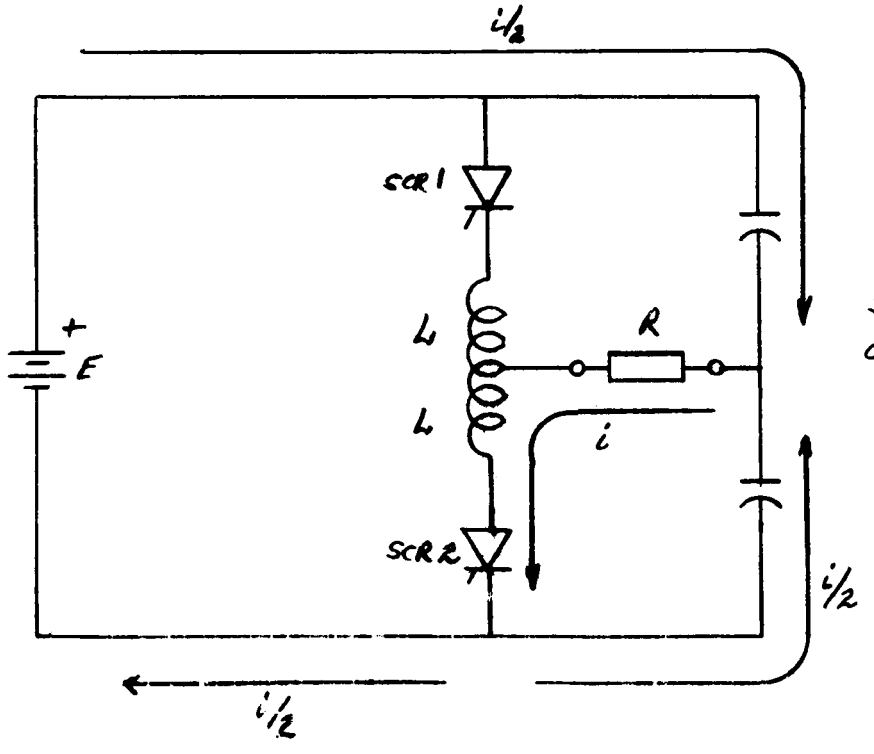


FIG. I-4

SCR 2
CURRENT PATHS

Fig. I-5

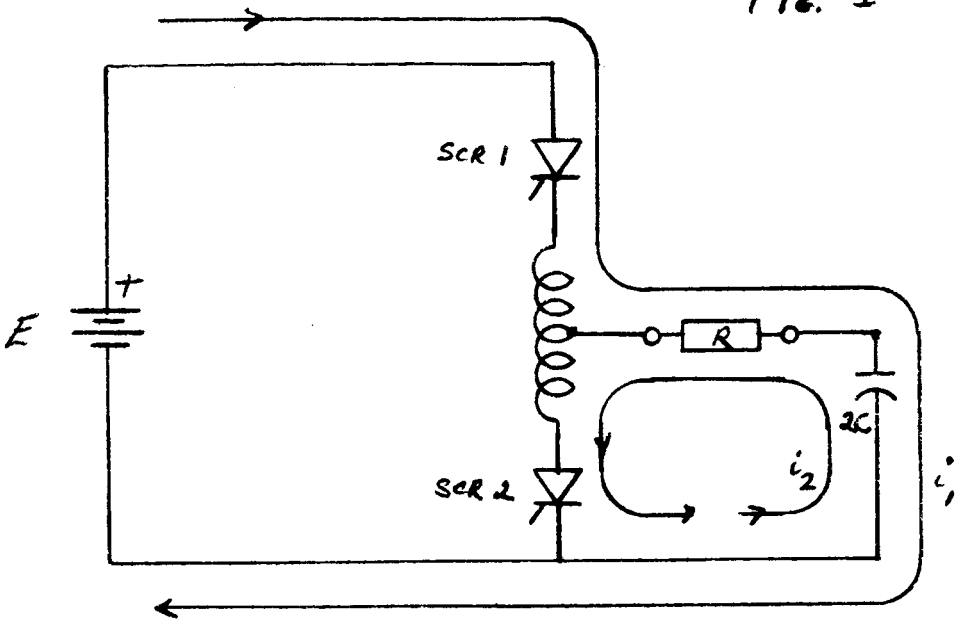


Fig I-5 Currents With Unsplit Load Capacitor

FIG. I-6

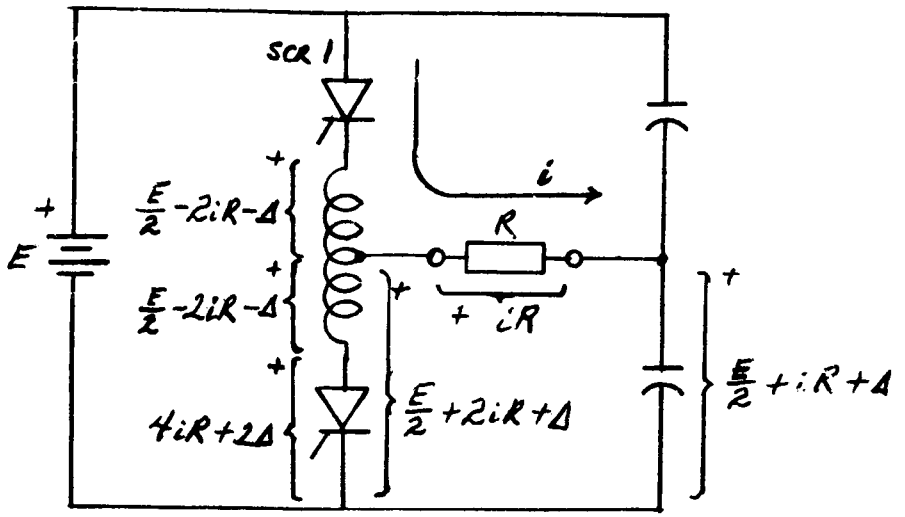
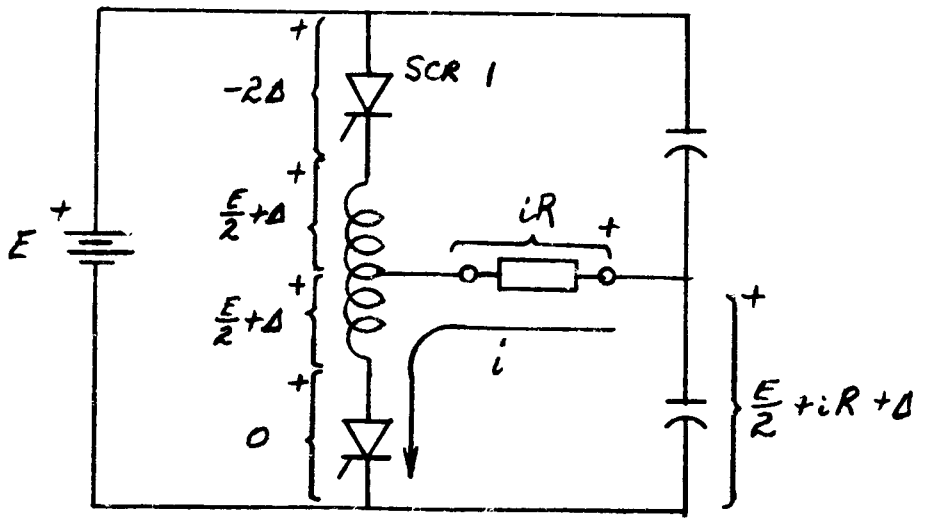


FIG. I-7



COMMUTATION OF SERIES INVERTER

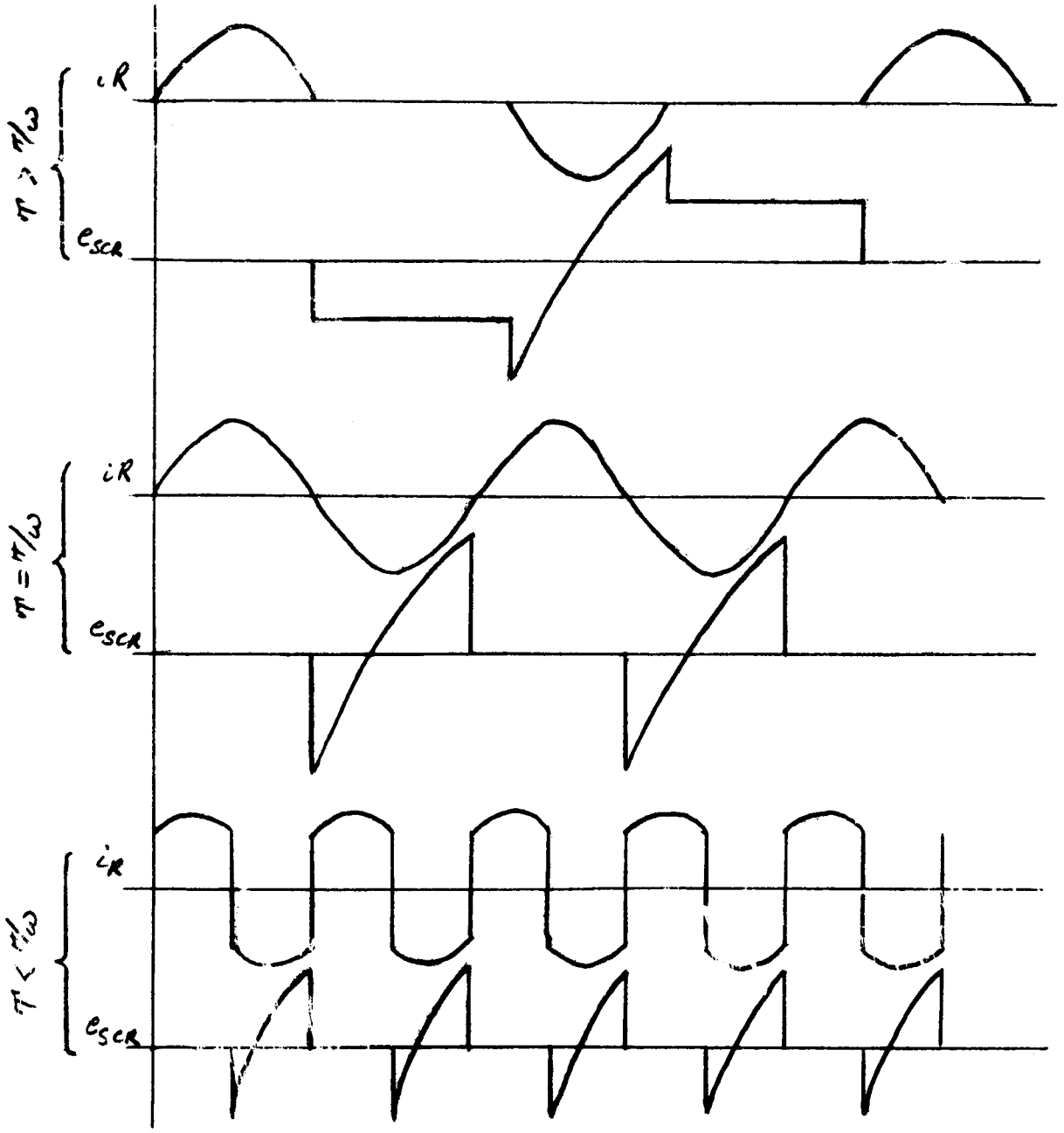


FIG. I-8 SERIES INVERTER OPERATION MODES

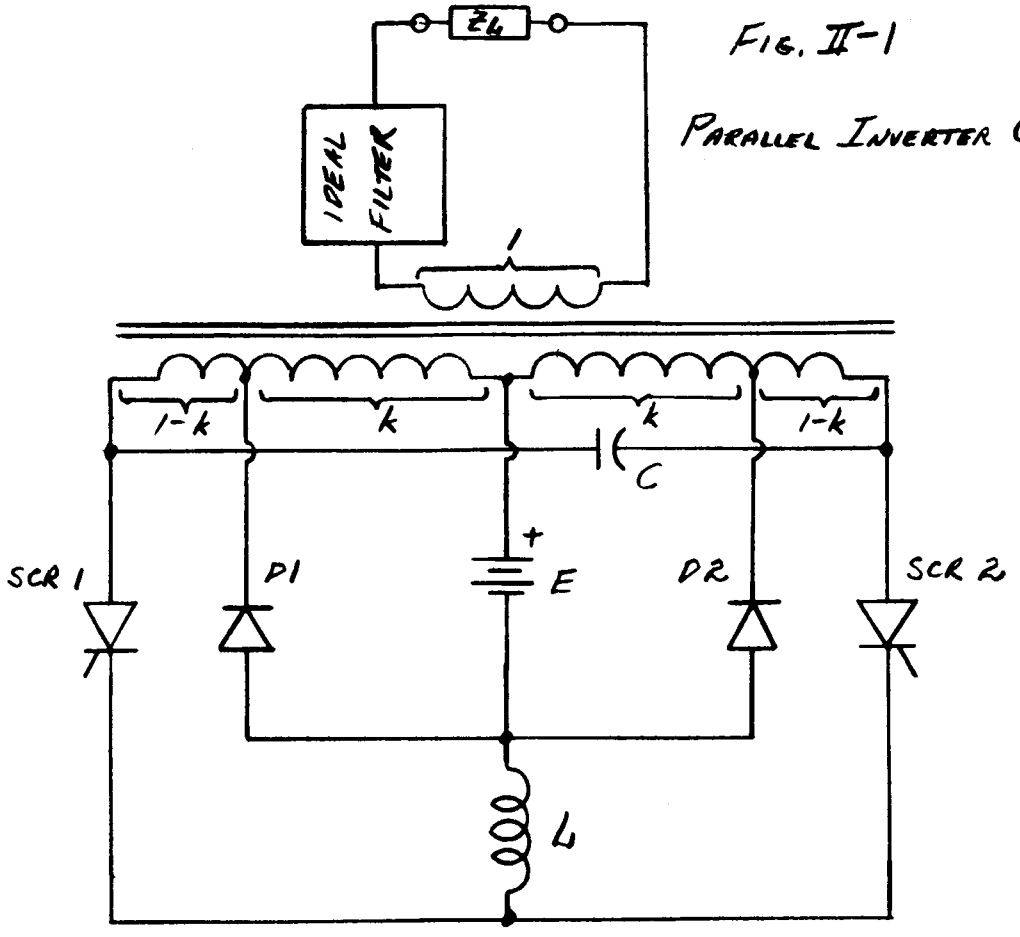


FIG. II-1

PARALLEL INVERTER CIRCUIT

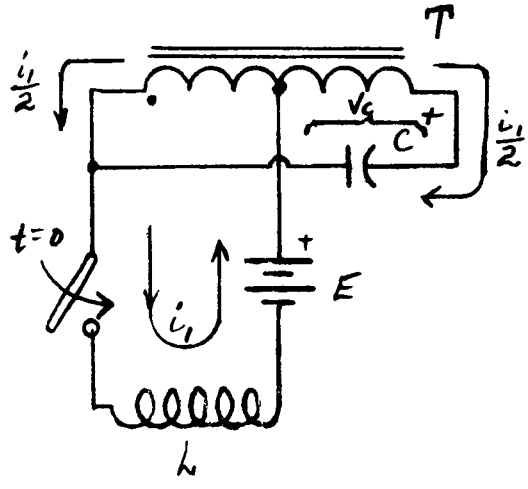


FIG. II-2

EQUIVALENT CKT. OF II-1

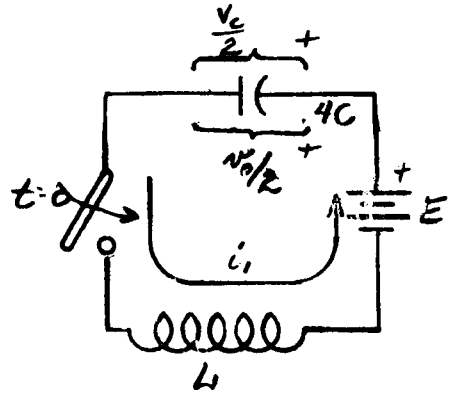


FIG. II-3

EQUIVALENT CKT. OF II-2

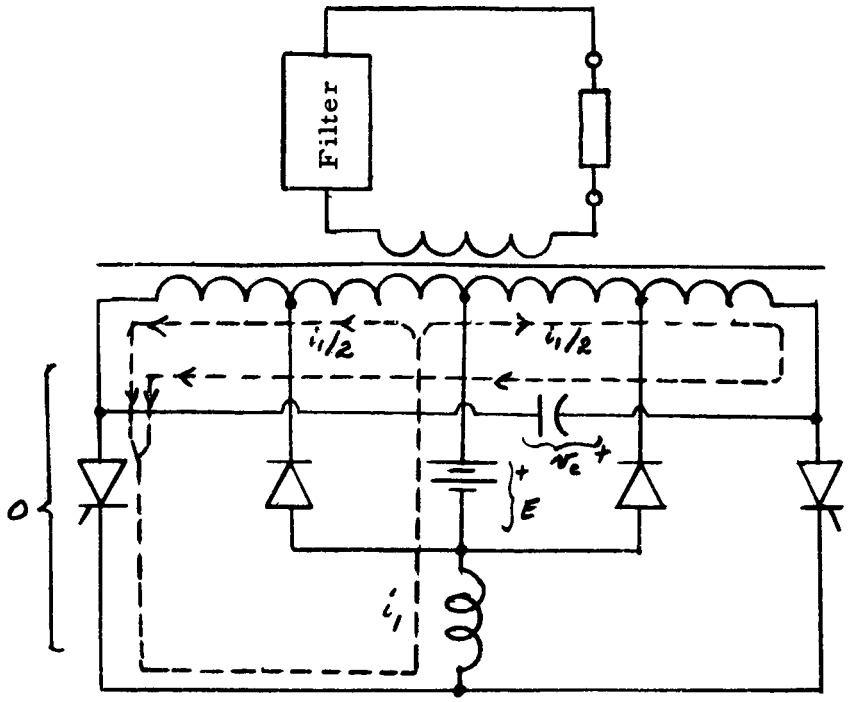


FIG. II-4 CAPACITOR CHARGE CYCLE: $v_c < 2E/k$

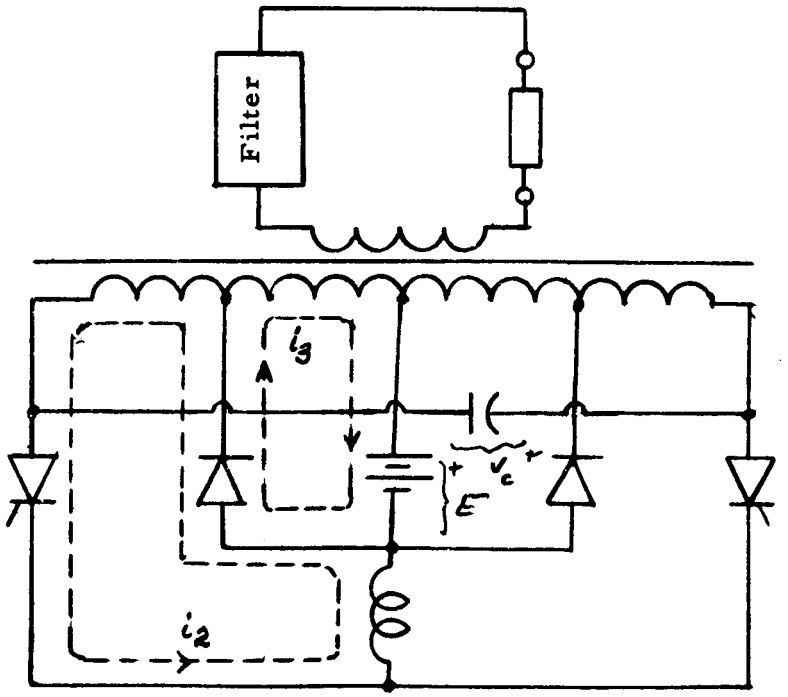


FIG. II-5 CAPACITOR CHARGE CYCLE: $v_c = 2E/k$

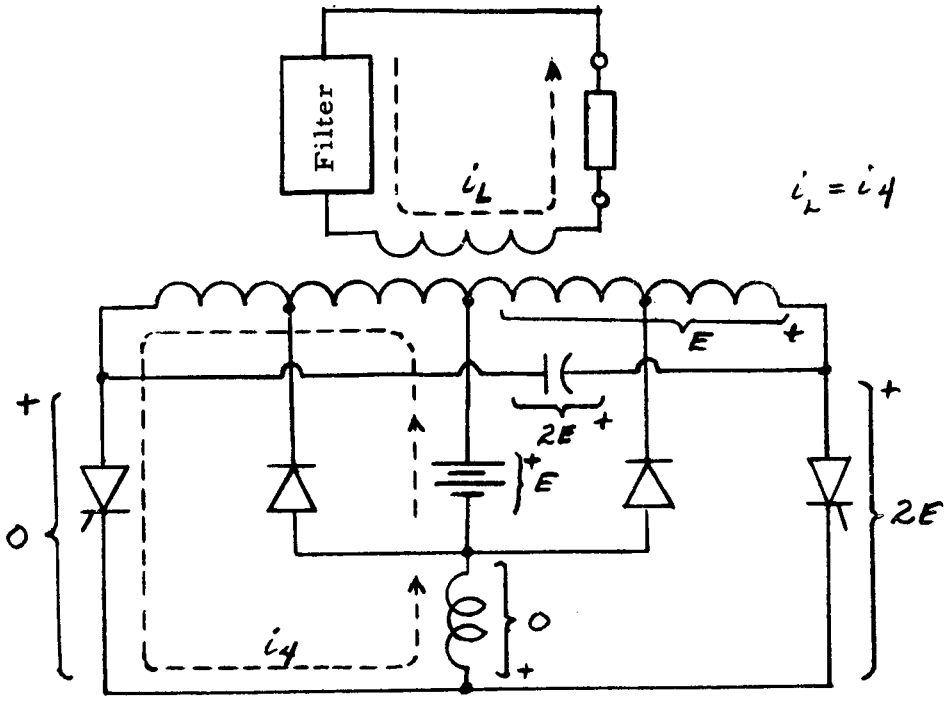


FIG. II-6 CIRCUIT IMMEDIATELY BEFORE COMMUTATION

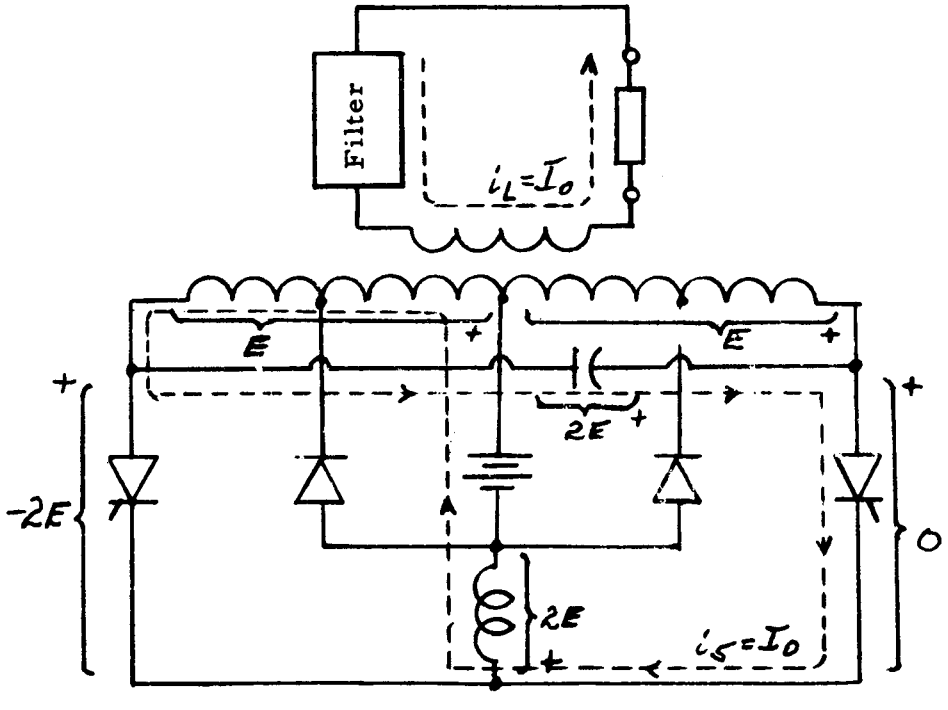


FIG. II-7 CIRCUIT IMMEDIATELY AFTER COMMUTATION

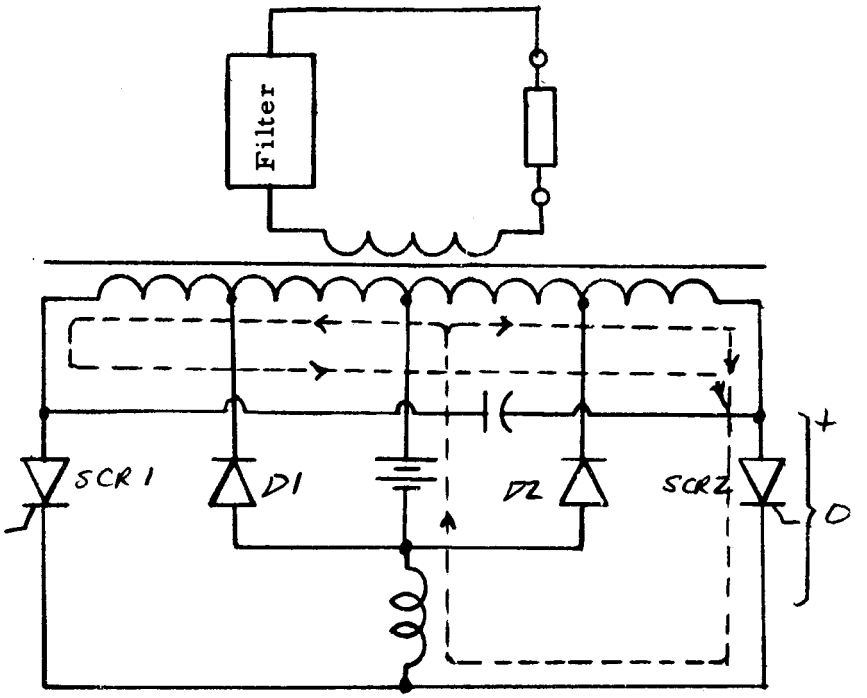


FIG. II-8 CAPACITOR CHARGING CURRENTS IMMEDIATELY AFTER COMMUTATION OF SCR 1 (TURN-ON OF SCR 2)

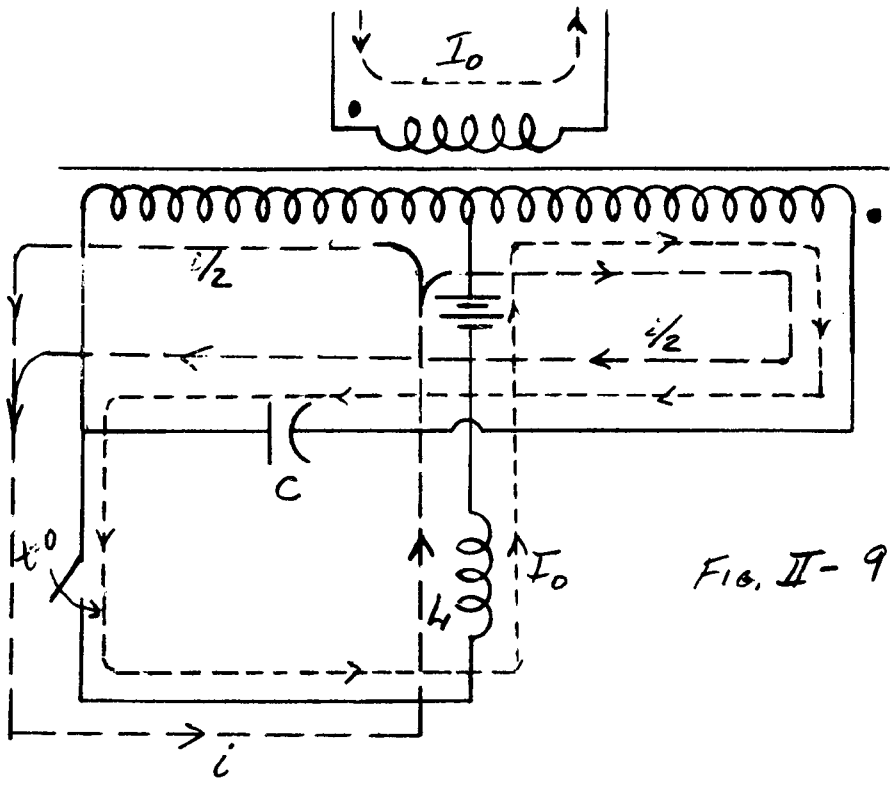


FIG. II-9A

CIRCUIT AT INSTANT OF TURNING ON OF SCR 1.

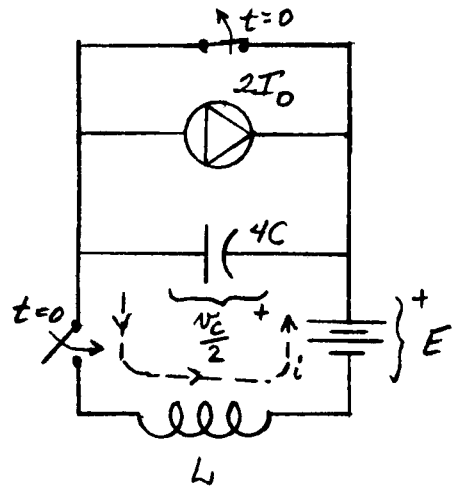


FIG II-9B

EQUIVALENT CKT. OF FIG. II-9A

STARTING AND STEADY STATE WAVEFORMS
McMURRAY-BEDFORD INVERTER RESISTIVE LOAD (WITH TUNED FILTER)

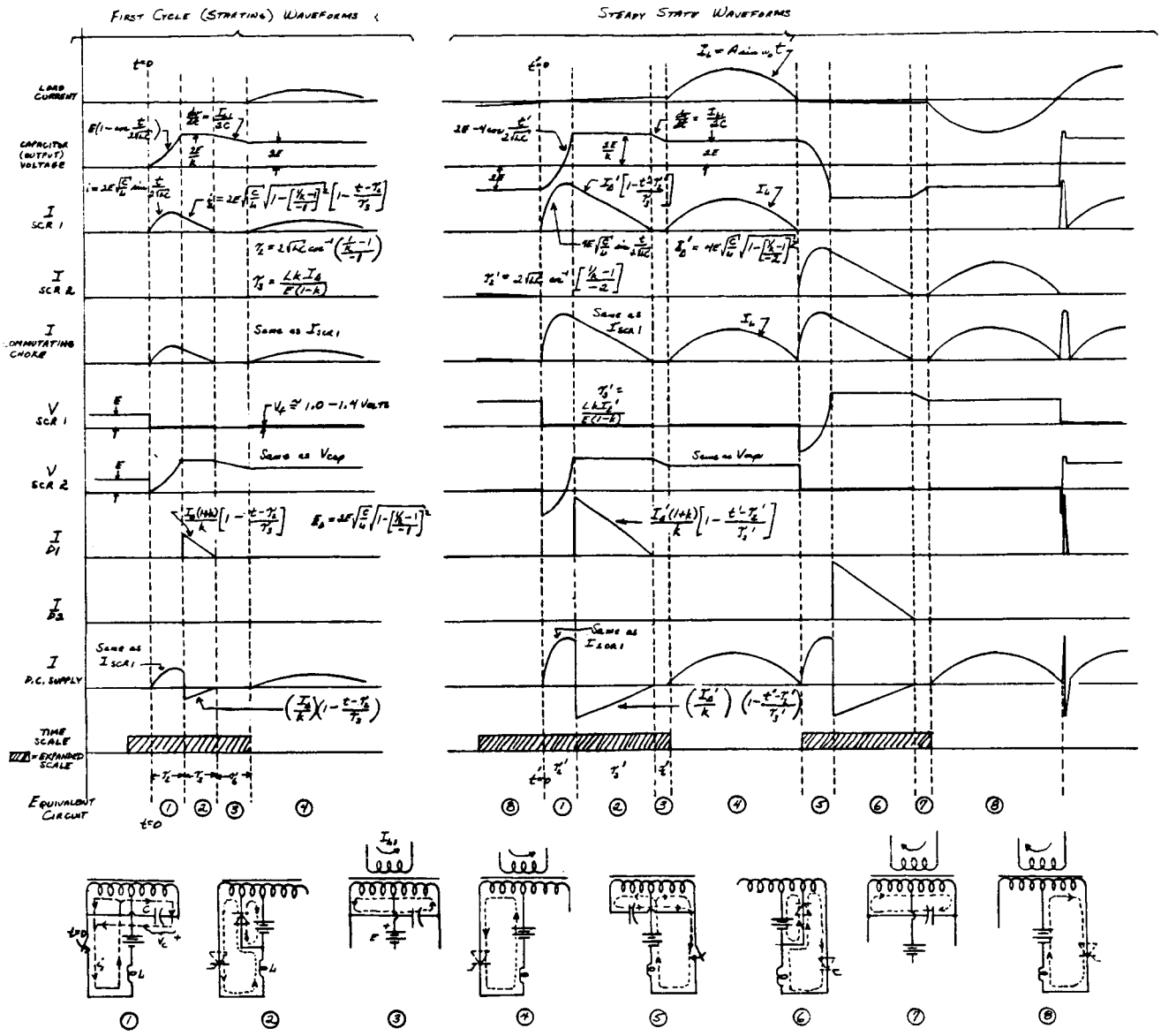
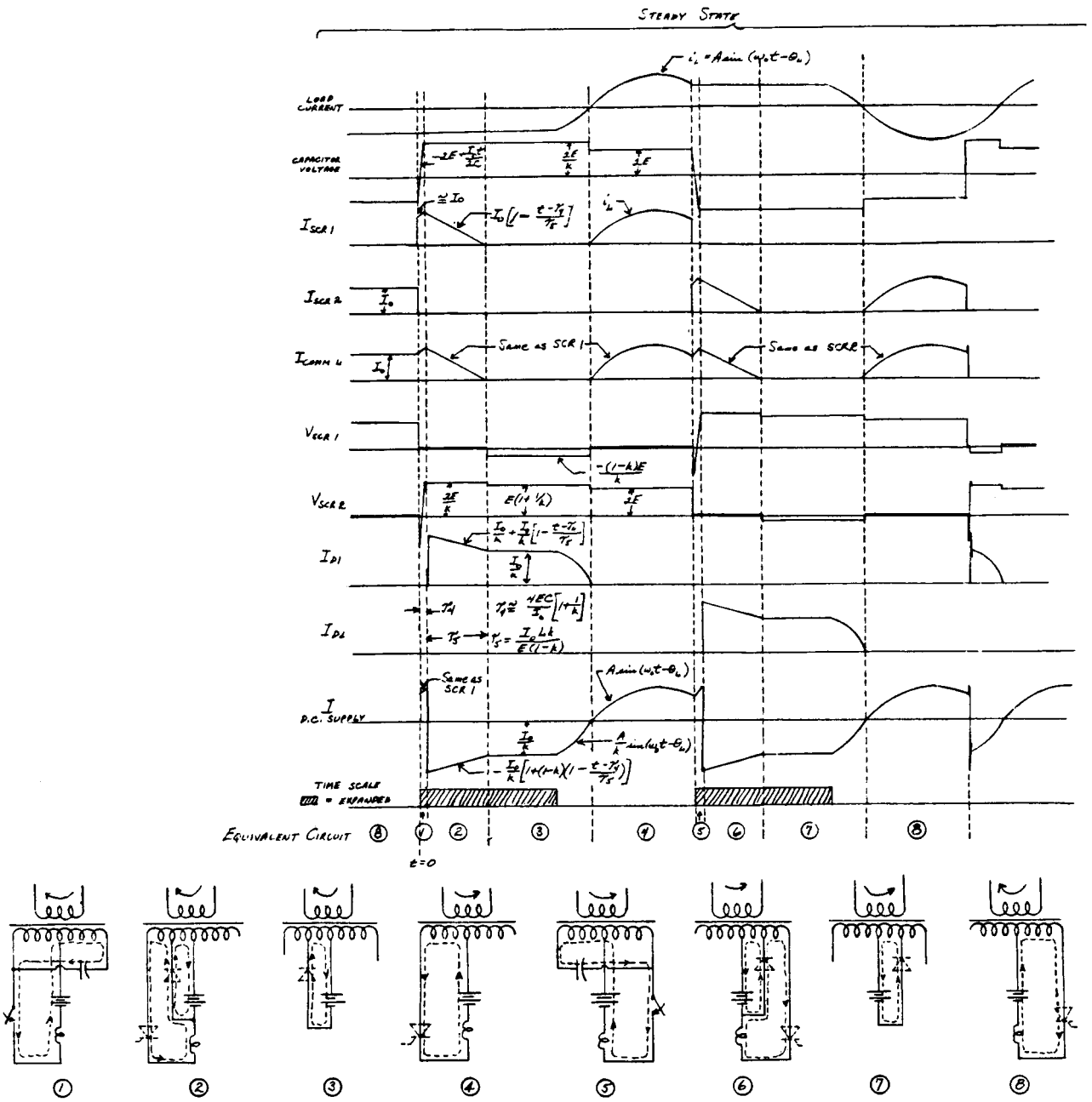


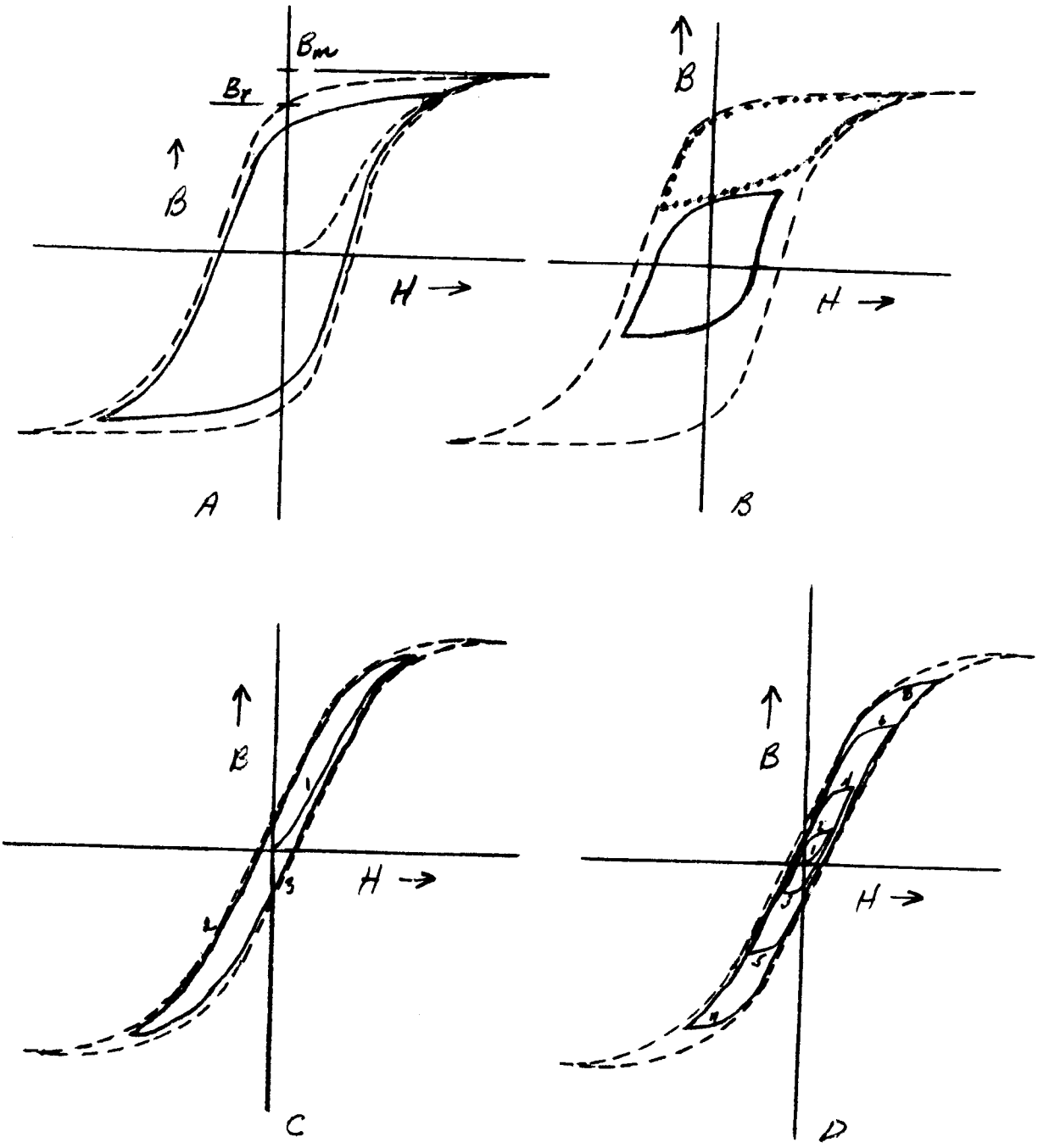
FIGURE II-10

McMURRAY-BEDFORD INVERTER WAVEFORMS INDUCTIVE LOADING



NOTE: STARTING WAVEFORMS FOR THIS CIRCUIT ARE THE SAME AS FOR THE RESISTIVE LOAD (FIG. II-10)

FIGURE II-11



DYNAMIC HYSTERESIS LOOPS – OUTPUT XFMR CORE

FIG. II-12

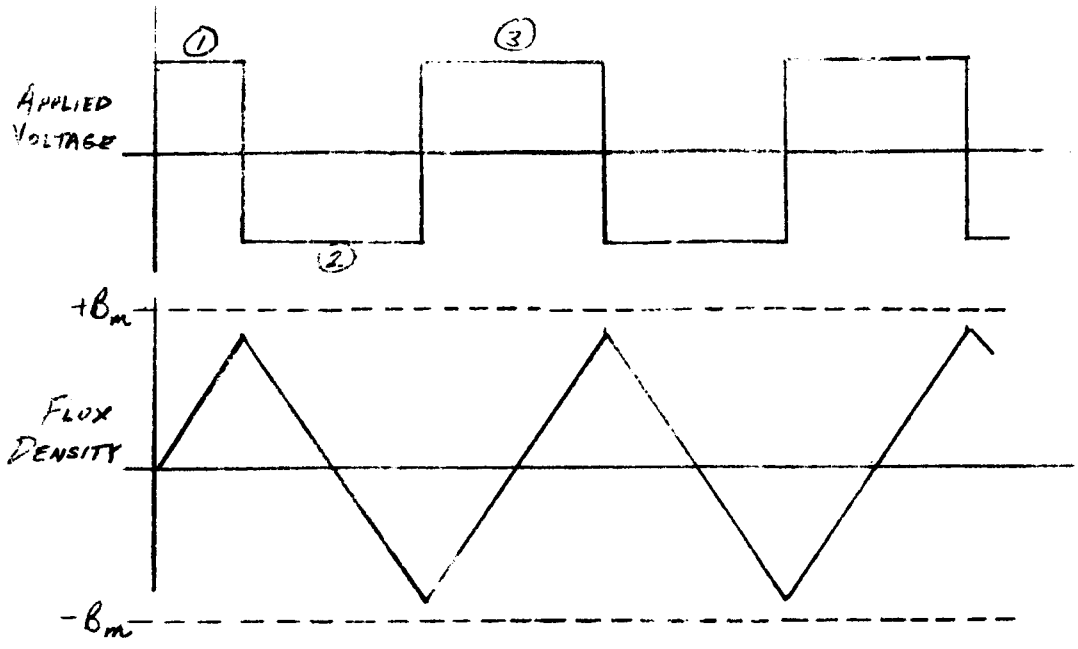


FIG. II-13A QUARTER CYCLE STARTING WAVEFORMS

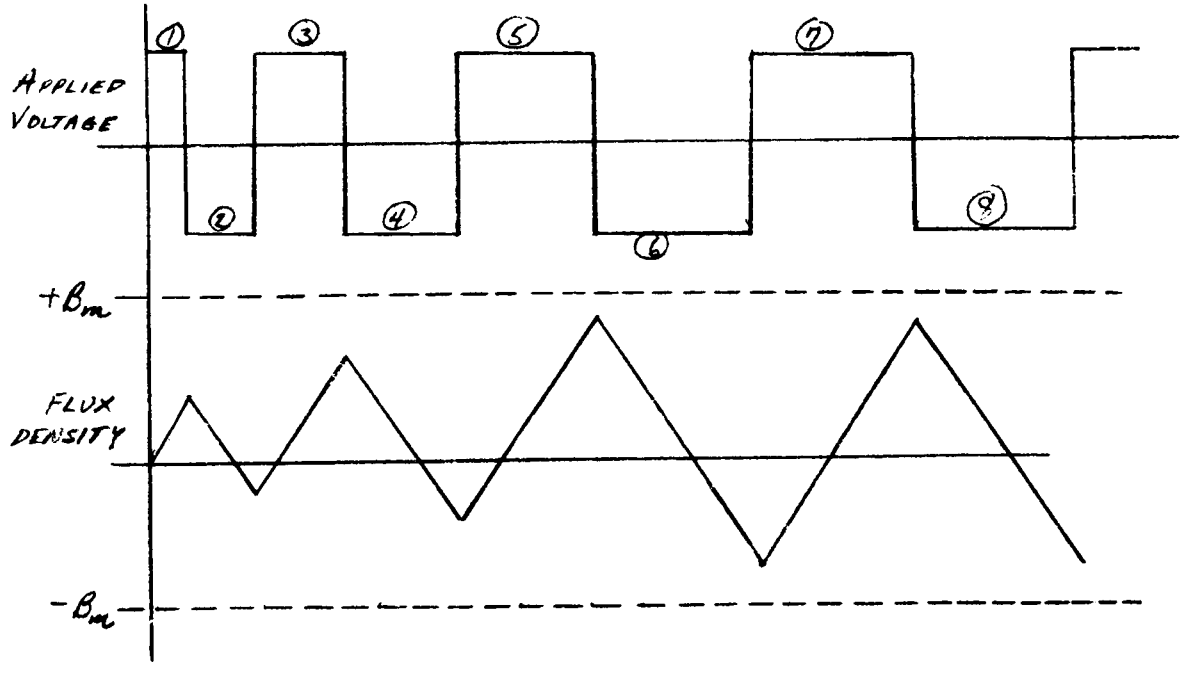


FIG. II-13B HIGH FREQUENCY STARTING WAVE FORMS

Study of 3200~Inverter Configuration

With this background of the types of circuits available, along with their significant characteristics, such as output voltage waveforms, allowable loads, and output variation with load etc., a study can be made of the possible approaches to any of the inverter groups described in the Methodology section. The problem of the 3200~10Kw inverter was considered first as it appeared to be the most difficult and no technique appeared to offer a clear advantage. The approaches considered (cataloged according to the basic power switching device) were:

1. Power transistors (Germanium and Silicon)
2. Silicon controlled rectifiers (SCR)
3. Gate controlled switches (GCS)

The merits and disadvantages of techniques utilizing these devices will now be discussed.

I Power Switching Devices

1. Power Transistors

The germanium transistor has the lowest forward voltage drop of all the devices listed (as low as 0.45 v @65A for 65 amp devices of suitable voltage rating). The drive requirements are moderate, being less than those of silicon transistors but greater than those of SCR's or GCS's. The speed of the devices at the higher current ratings (50A) is adequate to allow operation in the switching mode at 3200 cycles without excessive switching losses: (the switching losses are no more than three times the

forward conduction losses.) However, transistors suitable for operation with the pulse modulation techniques (with their minimum square wave operating frequency requirement of approximately 5 x the fundamental frequency) are available only in silicon. The allowable junction temperatures of germanium power devices generally are 110°C.

Considerations in the use of silicon transistors are approximately the same as those of germanium transistors with the differences that with silicon:

1. The maximum junction temperatures are 175-200°C, allowing higher ambients and/or device dissipation.
2. The forward losses are about double and the drive losses four times those of germanium units.
3. Available switching speeds are about twice as fast as those obtainable with germanium (in comparable sizes) with extremely fast switching ($\leq 0.1\mu$ sec) being obtainable in the lower ranges. (10A)

To handle the 10 Kw load, the number of transistors of either type that would be required can be determined by a few simple calculations.

For the first example, a system which utilizes a pulse modulation technique with a common square wave inverter was considered. A block diagram of the power section of such a system is shown in Figure 1-1.

Since the peak collector current is generally the limitation in the application of transistors to switching-type inverter circuits, and specifications require the device to handle 200% of rated current, the maximum average power output of the above system is 2 x 10 = 20 Kw. Assuming an overall efficiency of 90% (at full load) and allowing for a minimum battery voltage on a nominal 28 volt

system of 22.4 volts, the input current will then be $\frac{20 \times 10^3}{(.9)(22.4)}$ = 1000 amp. (If the same inverter is used to supply the a.c. power for all three modulators, as it is in this case, the instantaneous power requirements for the three individual phases will tend to cancel one another; in the case of a balanced load, this cancellation will be exact.) At 10A/transistor, this will require an absolute minimum of 100 transistors in parallel for each switch in the inverter circuit. Since a minimum of 2 switches is required (a typical circuit is shown schematically in Figure 1-2) a total of at least 200 transistors would be needed for the square wave inverter section of such a scheme. This is using high speed transistors with a maximum collector current of 10A each.

Needless to say, this appears to be unreasonably large from a reliability point of view. Using the larger but slower 50A transistor, the number could be cut to 40 total, but the switching dissipation of 130 watts/transistor (at 15,000 cps, 200% load) would be out of bounds; the switching stage efficiency at 100% load would be only 78%. However, some technique which allowed the switching to be performed when the collector current was at or near zero might reduce this loss to an acceptable value. This pulse modulation inverter would require additional semiconductors in the modulators (although this might be performed with magnetic circuitry); these would probably be SCR's or GCS's due to the voltages involved and the a.c. operation.

Another approach would be to perform the inversion at 3200 cps, thus reducing the switching losses over the pulse modulation schemes. (This would mean

using an inverter of the quasi-square wave or stepped wave types.) If the inversion were handled by three separate inverters, one for each output phase, the average current handled by each inverter section would have a maximum of 1000/3 = 333 amp. This is calculated on the basis of a 200% load, minimum battery voltage (worst case) and an efficiency of 90%. Thus, the peak current in each phase input could rise to $333\frac{\pi}{2}$ = 520 amp. Therefore, each side of each phase switch would need a minimum of 520/50 $\cong$ 11 transistors, for a total of 66 transistors for a 3 $\emptyset$ system. The switching losses in this example would be less than 1/5 of those calculated for the previous circuit because

1. The switching is done at a lower frequency (1/5 that of the pulse modulation system) and switching losses are directly proportional to frequency for the ranges considered.

2. In normal operation, the switching does not occur at the times of maximum collector current, as it does in the pulse modulation scheme. (Switching losses are directly proportional to the collector current at the time of switching.)

Figuring losses for the worst case (200% load, switching occurring at peak collector current) the following results are obtained with a Bendix 2N2358 germanium 50A high speed switching transistor:

Switching losses (I_C = 50A, t_r+t_f = 16μsec)	25.6 watts
Reverse losses	1 watt

Forward losses	11.2 watts
Drive losses	3.7 watts
Total	41.5 watts

With a thermal resistance of 0.5°C/watt and a maximum junction temperature of 110°C, the transistor mounting base must be held to 89°C or below.

This is a transient condition lasting for only 5 sec; the maximum steady state dissipation is less than 1/2 of the amount calculated; the maximum mounting base temperature under steady-state conditions will be at least 100° C.

For the same worst case example as calculated for the germanium transistors, the losses in a silicon transistor are:

Switching losses (at I_C = 50A)		13 watts
Reverse losses		1 watt
Forward losses		31 watts (calculated for Silicon Transistor Corp #2107)
Drive losses		15 watts
	Total	60 watts

With a thermal resistance of 0.5°C/watt, the maximum junction temperature allowed with this unit = 200 -.5 (60) = 170°C. This is considerably higher than the 89°C permitted by the germanium devices.

Both these calculations have been performed for the worst case; at only 100%

load, the switching losses would be about 1/2 those calculated above, and the forward losses would be reduced by a factor of four. (Since a saturated transistor approximates a fixed resistance, the forward losses vary as the square of the current). Thus, the full load losses for the germanium transistors would be less than 20.3 watts and the silicon loss would be less than 30.5 watts.

Even at these rates, the switching efficiency of the silicon transistor power stage alone will be only $\frac{10,000}{10,000+66\,(30.5)}$ = 83%. This value would improve with better transistors (i.e. faster, lower leakage, lower saturation resistance, higher gain) and/or circuit changes. Possible circuit changes include techniques for optimizing the switching pattern, reducing the current and/or voltage at the time of switching, or reducing the effective switch resistance by connecting additional units in parallel. Drive losses can be reduced by providing a drive proportional to the instantaneous collector current rather than a square wave drive adequate for the largest collector current (though at the expense of increased complexity). Because of the large numbers of units which may be operated in parallel, these circuits offer possibilities for increasing reliability through redundancy without significantly increasing the circuit complexity. On the other hand, because of the large number of elements, some form of redundancy will probably be necessary in order to maintain the reliability.

Any of the various parallel switching circuits discussed earlier could be used with these transistors; however, the bridge circuits would not be desirable at the 28 volt level considered here because they would require twice as many transistors (and have about twice the semiconductor losses) as the parallel inverter with center-tapped transformer. As the input voltage increases, the number of transistors required in parallel to handle the input current decreases; thus higher input voltages are advantageous. However, as the input voltage goes too high, the bridge circuits would become necessary because of the voltage limitations of available transistors. (Other conditions remaining equal, the transistors in a bridge are subject to only one-half the voltage as those in a center-tapped transformer arrangement.)

2. Silicon Controlled Rectifiers

SCR's have the advantage of being able to handle very large currents, both on continuous and pulse bases. They are available in ratings up to 400A rms, 250 A average, with peak current capabilities in the thousands of amperes. They are also available in high voltage ratings (up to 1300 volts). Their forward voltage drop is slightly higher than that of silicon transistors and tends to remain constant as the current is increased. (Transistor drop (saturated) is almost a linear function of current and can be represented as a resistance.) However, the fact that SCR's must be commutated off by an external source adds circuit complexity and, in particular, results in additional losses.

The amount of the commutation losses as compared to the (reflected) load current loss in an inverter circuit serves as a good indication as to the suitability of the circuit for the intended operation. These losses can be computed for the first circuit under consideration (the McMurray-Bedford circuit) as follows:

The first problem is to determine the value of the commutating capacitor since it determines the maximum current that can be commutated as well as many of the circuit currents, and except for the selection of the basic circuit itself, is the initial step in inverter design.

Assume the maximum current to be commutated is I_o amperes. (This will correspond to a 200% load at a power factor which places the peak of the load current pulse at the time when commutation occurs.) Let the minimum supply voltage be E. Then, the capacitance required to provide a turn-off-time of t_o is obtained by a rearrangement of equation II-30 to obtain:

$$C = \frac{I_o t_o}{2E} \qquad (1\text{-}1)$$

The next problem is to evaluate the currents in the circuit (and particularly in the SCR). For the McMurray - Bedford circuit, much of this analysis had already been done in Appendix II, and reference will be made to that. For negligible current at the time of commutation (which could occur at 100% resistive load with a tuned filter, where the sinusoidal load current would be in phase with the inverter switching stage output, and hence be going through zero at the instant of commutation) the SCR

current is given by equation II-2, which for the steady state case where $v_o = -2E$, has the value

$$i = 4E\sqrt{\frac{C}{L}}\sin\frac{t}{2\sqrt{LC}} \qquad (1\text{-}2)$$

This, of course, is subject to the restrictions imposed in the derivation of equation II-2; in particular, it applies only for $0 \le t \le \tau_2$ where τ_2 is given by equation II-6. If K, the reactive tap fraction (refer to Figure II-1 and the discussion on page 57) is set at 0.8, then the time required for the current trapped in the commutating choke to reach zero is given by equation II-10. With $v_o = -2E$, $k = 0.8$ and using the approximation $\sqrt{1-(1/8)^2} \cong 1$, this time (τ_3 in equation II-10) equals $16\sqrt{LC}$ seconds. The current waveform in the SCR (and commutating choke) due to the commutation circuit is then as shown in Figure 1-3. The time at which the waveform changes from a sinusoid to a linearly decreasing ramp is given by equation II-6 as

$$\tau_2 = 2\sqrt{LC}\cos^{-1}\left[\frac{E/k - E}{-(E - \frac{v_o}{2})}\right] = 2\sqrt{LC}\cos^{-1}\left(-\frac{1}{8}\right) \cong 3.4\sqrt{LC} \qquad (1\text{-}3)$$

The average value of this current pulse (averaged over a half cycle of the operating frequency) can be easily determined as described below. (Average currents are used in these calculations because the voltage drop across the SCR is fairly constant with current, thus making the average current a better indicator of SCR losses than rms current. The same is true for diode losses.) Approximating the exact current waveform (shown in

Figure 1-3 as a solid line) with a triangular current waveshape (shown dotted in Figure 1-3) of height equal to the actual current maximum and base equal to the total time required for the pulse, the average current in one SCR (during the half cycle that it is conducting) due to commutation currents only is $I_{avg} = \left(\frac{I_{peak}}{2}\right) \frac{\text{pulse length}}{T_o/2}$ (1-4)

where T_o is the period of the fundamental frequency of operation of the inverter. Substituting the values of peak current (equation 1-2) pulse length (equation 1-3) and fundamental frequency $f_o = 1/T_o$ into this equation, there results:

$$I_{avg} = \frac{\left(4E\sqrt{\frac{C}{L}}\right)\left(3.4\sqrt{LC} + 16\sqrt{LC}\right)}{T_o} = 77.6 E f_o C \qquad (1\text{-}5)$$

Substituting the value of C from equation 1-1 into equation 1-4 and realizing that, if I_o is the peak current during the 200% overload condition, the average current during the conduction period for each SCR at the 100% load condition will be

$$I_{avg\ (load)} = \frac{I_o}{2} \times \frac{2}{\pi} = \frac{I_o}{\pi} \qquad (1\text{-}6)$$

Then, the ratio of the average SCR current due to all causes $\left[I_{avg\ (comm)} + I_{avg\ (load)}\right]$ to the average current due to the (reflected) load current only $\left[I_{avg\ (load)}\right]$ is $\frac{I_{avg\ (comm)} + I_{avg\ (load)}}{I_{avg\ (load)}}$

$$\frac{77.6\, f_o \left[\frac{I_o\, t_o}{2E}\right] + \frac{I_o}{\pi}}{I_o/\pi} = 122\, f_o\, t_o + 1 \qquad (1\text{-}7)$$

For the case of the 3200 cycle inverter, and using a 20 μsec turn-off-time, this ratio becomes $1 + 122\,(3.2 \times 10^{3})\,(2 \times 10^{-5}) = 8.8$ Thus, with total SCR losses 8.8 times the losses due to the reflected load current only, the McMurray -Bedford inverter is not suitable for efficient operation at this high a frequency. (Less than 1/8 of the total switching device loss arises from providing power to the load.)

A more efficient (and complex) parallel inverter (the McMurray circuit) is shown in Figure 1-4. Here, the four additional SCR's Q3, 4, 5, and 6 are used to achieve commutation without turning on the other power switching SCR. This allows quasi-square wave operation. However, the main purpose of this circuit is the reduction of commutating losses brought about by the fact that the commutating energy merely moves back and forth through the tuned circuit to achieve commutation instead of being largely dissipated and later resupplied from the d. c. source each half cycle. With this improvement, the commutating losses in the SCR's are considerably reduced from those of the McMurray - Bedford circuit.

The operation of this circuit can be analyzed as follows: Assume SCR 1 (Figure 1-4) is on and SCR 4 and SCR 5 have been simultaneously gated on so that C_c has acquired a charge such that the positive side of C_c is the one connected to L_C. Then, when it is time to turn off SCR 1, SCR 3 and SCR 6 are simultaneously gated on, and C_c discharges through L_c, SCR 3, SCR 6, the load and, when the discharge current has built up to a

high enough value, through D_1, causing a reverse bias of about 1 volt to appear on the anode of SCR 1. With proper choice of components, this reverse bias can be maintained for the required turn-off-time.

A portion of the current waveform produced by the turning on of SCR 3 and 6 is shown in Figure 1-5. Here again, I_o is the maximum current which the circuit is designed to commutate and t_o is the minimum circuit provided turn-off-time. With L_c and C_c chosen to resonate at a frequency with period 4 t_o, and provide a peak current of $\sqrt{2}\, I_o$, the current taken by the resonant circuit will be greater than I_o for a period of t_o. This resonant current, which flows through SCR 3 and SCR 6, has an average value (when averaged over 1/2 period of the fundamental inverter output frequency) of

$$I_{avg\,(comm)} = (\sqrt{2} I_o)\left(\frac{2}{\pi}\right) \times \frac{2t_o}{T_o/2} = \frac{8\sqrt{2}}{\pi} I_o t_o f_o \qquad (1\text{-}8)$$

where, again $f_o = \frac{1}{T_o}$ Since current flows through two SCR's, the ratio of total losses to losses due to forward current equals

$$\frac{\frac{I_o}{\pi} + \left[\frac{8\sqrt{2}}{\pi} I_o t_o f_o\right] 2}{I_o/\pi} = 1 + 16\sqrt{2}\, t_o f_o \qquad (1\text{-}9)$$

For a 3200ν inverter with minimum turn-off-time of 20μsec, this value becomes 2.45. This results in the 100% load SCR losses for this inverter circuit being equal to those of a (silicon) transistorized inverter and hence about 1 1/2 times those of a germanium transistor inverter.

However, the SCR circuits also have additional losses due to the commutating currents flowing in the commutating choke and capacitor, reactive diodes, and output transformer primary. The McMurray circuit is also superior to the McMurray-Bedford inverter in these respects, and thus has much improved commutation losses over the McMurray-Bedford circuit. This loss is not obtained without penalty, however. The number of SCR's per power stage has increased from 2 to 6 and the drive circuitry required has increased in complexity. (On the other hand, this circuit does allow non-zero clamped quasi-square wave operation. See page 30 for a discussion of zero clamping.) Also, in the McMurray-Bedford circuit, a current to commutate greater than the design maximum (I_o) simply decreases the available turn off time by a proportional amount. For example, if t_o is available with a current of I_o, then $\frac{t_o}{1.5}$ is the available turn-off-time with $I = 1.5\ I_o$. With the safety margin in the turn-off-time provided, (It is anticipated that 12μsec turn-off-time SCR's would be used, for example, in a circuit designed to provide a minimum of 20 μsec.) the circuit would still operate under this condition. However, in the McMurray circuit (designed for t_o seconds at a current of I_o) since $1.5 I_o > \sqrt{2} I_o$ (where $\sqrt{2} I_o$ is the absolute maximum of the current pulse taken by the commutator circuit) there would be absolutely no turn-off time provided by the circuit and circuit failure would be certain.

The series type inverter possesses the advantage of not requiring additional commutation devices; for the proper load range, it is self-commutating. This "proper" load requirement (which restricts the load resistance to below a certain value) can be circumvented by putting an appropriate capacitor across the load terminals. This allows operation at no load. However, the input frequency will still change considerably under these conditions, requiring that the output of the inverter be filtered in the same fashion as the parallel inverters. The current through the shunt capacitor (which may be considerable if the shunt capacitor is also required to tune out a possible inductive component of the load) results in increased losses. In addition, clamping schemes which operate in a fashion similar to the reactive diodes of the parallel inverter are needed to suppress excessive voltages which would otherwise occur at no load or short circuit operation.

Reports [3] indicate an efficiency of only about 70% can be expected for series inverters which must operate over a 3:1 load range; our requirements are even more difficult than that, operation to no-load being required. Also, the series inverter suffers from the same reliability drawback that occurs with all SCR inverters -- one unsuppressed noise pulse from any source can cause a misfire and shut down the inverter, unless some redundant methods are used to allow shutdown of a stage or the inverter is automatically restarted. In either case, the extra circuitry

required to account for the misfire is added components which increases weight and decreases reliability. Also, the higher losses in SCR's as compared to germanium transistors and the recent increases in maximum operating junction temperatures of germanium transistors (to 110°C, as compared to the 125°C allowable for SCR's) result in the two devices requiring about the same mounting base temperature. Thus, from a thermal point of view, SCR's possess little advantage over germanium transistors, and are less efficient. Although the number of transistors required for the power switching stage of the 10 KW unit is fairly large, because of the fact that they are essentially connected in parallel, redundant techniques will be fairly easy to apply. Also, the 10 KW is at the high power end of the anticipated sizes; the lower power units of the same type (the range extends down to only 2 KW) will require fewer transistors (the number in the switching stages is proportional to the maximum power output desired).

From a weight point of view, the additional weight required by the many transistors over a few SCR's would be expected to be made up by the elimination of the commutating capacitors and chokes, as well as the reduction in the sizes of the output transformers and heat sinks made possible by the increased efficiency of the transistorized devices and absence of the high peak currents associated with SCR commutation.

The "paper" reliability of the SCR circuits with their smaller parts count can be made up by easily applied redundancy techniques to the switching stage transistors. Safety margins on transistor voltages can generally be introduced without any weight or efficiency penalties; increasing the turn-off-time margin in an SCR inverter means increasing the size (and weight of the commutating capacitor and there by increasing the losses in the circuit components responsible for charging it up.

3. Gate Controlled Switches

The gate controlled switch is similar to the SCR except that it can also be turned off at the gate. These are presently available only in low current ranges (6A) with some improvement expected in the near future.

Since they appear to be restricted to current ranges below those of transistors and have a higher forward drop (2v @ 5A) they do not appear advantageous for this inverter. However, their combination of high voltage ratings and improved turn off (over SCR's) would favor them in inverters operating at higher voltages where currents are lower (for a given power rating) and transistors unavailable.

A typical circuit employing the gate controlled switch is shown in Figure 1-6. It is very similar to the SCR circuits described earlier (Figure 4) with the exception that the commutating choke has been eliminated and the commutating capacitance has been split, made smaller, and connected from gate (of one GCS) to anode (of the other GCS). A resistor is also inserted in series with it to limit the peak reverse gate current to a safe value. The operation of this circuit is akin to that of a conventional flip-flop. A positive pulse coming in to the gates turns on one GCS and leaves the other on. The sudden drop in anode voltage of the first GCS is coupled through R and C to the gate of the other GCS, turning it off. The next positive pulse reverses the process, turning on GCS 1 and turning off GCS 2. The output of this circuit is a square wave.[7]

Like the SCR, the GCS has a turn-off-time which varies with load and temperature and during which, for the GCS, its gate must be held negative. Also, as with SCR circuits. GCS inverters can mis-fire, ending up with both power switches on and the circuit inoperative.

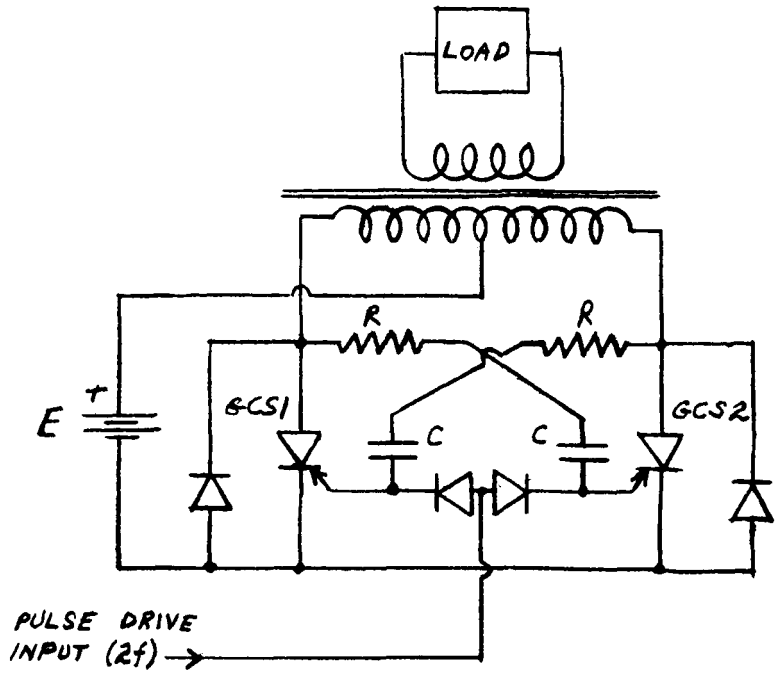


FIG. 1-6 GATE CONTROLLED SWITCH INVERTER CIRCUIT

II Paralleling Techniques

These initial considerations would appear to favor the transistor circuits because of weight, efficiency and reliability. However, the paralleling problem in transistor circuits must be examined closely to see if it does not present other problems.

Paralleling techniques will now be investigated.

One method is to insert balancing resistors in series with one or more leads of each transistor. Unfortunately, the more effective this method is to be, the larger the resistors must be, and the greater the power wasted. The use of balancing reactors, though an efficient solution to the problem for the case of diodes, must be carefully analyzed for transistors because some of the simpler circuits can result in a voltage transients of 4E (where E is the battery voltage) appearing across the transistors for a short time due to the difference in the switching speed of the transistors.

An alternative to the use of balancing resistors or reactors to achieve current balancing when paralleling transistors (or SCR's) is to break up the output transformer into N smaller units (each with 1/Nth the secondary voltage rating of the original transformer) and connect the secondaries of these units in series to obtain the originally desired output. This technique is shown in the diagrams of Figure 1-7A and 1-7B. Since the same load current flows in all of the secondaries, the reflected load currents carried by all the transistors which are conducting at any given time are equal. This balancing is obtained at the expense of splitting up one large transformer into N smaller ones of the same total rating, a procedure that results in an overall increase in weight and losses in the output transformers. However, the primaries now need not be excited in all parallel; each stage can be turned on at a slightly different time to produce

a stepped output or synchronous switching waveform. Thus, the additional weight and losses required by the individual transformers can be partially offset by lower filter requirements due to the reduced harmonic content of the output of the switching stages, (and the absence of any additional components which would be otherwise required for balancing.)

Which technique is better will have to be decided on the basis of further studies comparing the weights and losses of the output transformer(s), balancing reactors (if used) and filters of the two systems and considering the complexity of the drive circuitry and ease of applying redundant techniques for reliability improvement.

III Voltage Regulation

Methods of voltage regulation will be considered next. Basically, there are three main techniques for regulating the output voltage of an inverter against variations in load and/or input voltage. These are:

1. Regulating the d. c. input voltage to the inverter stage. All techniques studied so far for this purpose have required at least one semiconductor in series with the main load current path. This places an upper limit on the efficiency of such regulators, and can result in relatively high losses when operating on low voltage systems. The number of semiconductors is also increased; the regulator would require at least half as many semiconductors (of the same type) as the total number in the power switching stages. The advantages of

d. c. regulation is that it provides an almost constant d. c. input to the power switching stages, thus allowing them to be optimized for only one input level. Input regulation also allows the use of complex waveforms for harmonic reduction without distortion problems caused by deviations from the ideal waveform brought about by the necessity to vary some parameter of the generated waveform to obtain voltage regulation. The filtering and inverter logic are also simplified if voltage regulation is performed on the input d. c., since the optimum spacing between steps of a multi-stepped wave can be maintained independently of the input voltage and load variations.

In view of the large currents required, and the relatively low voltage available for the 28 volt unit, it was felt that the d. c. regulation techniques were not suitable for this application.

2. Varying the form of the inverter output waveform in the switching circuit to vary the fundamental component of the switched output waveform. The quasi-square wave is a good example of this technique, although more complex waveforms are possible and may be desirable. Methods for voltage regulation by varying the phase between two generated waveforms to yield a variable vector sum are the most efficient from a semiconductor standpoint but require a larger output transformer capability than needed with other techniques.

This efficiency stems from the fact that at the lowest input voltage and heaviest load, where the input current is greatest, all the semiconductors are operated in phase and all contribute to the output power at all times. At higher input voltages, where the current demands are less, and the outputs of the separate power switches no longer in phase, at some portions of the cycle, one power switching stage will be supplying power to another stage, which is returning that power to their common source via reactive diodes. This circulated energy undergoes loss because it must pass through one transistor, one diode, and two transformers in its roundtrip. Thus, at higher input voltages, at least part of the time, losses occur in the semiconductors which do not result in any energy being transferred to the load. Also since the load voltage is less than the algebraic sum of the individual transformer voltages (because the load is a vector sum, and except for the low voltage high current operating point, the individual outputs are not in phase) a larger transformer capability than the load rating is required with this technique. (At 3200 cycles, this would not cause as severe a weight penalty as at lower frequencies.) The problem of wasted transformer capability can be solved by generating a quasi-square wave directly with the switching elements, rather than with phase shift techniques. This does require more complex control circuitry and additional semiconductors than the phase shift technique. The extra semiconductors are used as switches

to short the output transformer primary during the periods when neither power switching element is on. This is called zero clamping and avoids the type of waveform distortion shown in Figure 5K.

3. The unregulated a. c. (square wave) output of a switching stage can be operated on either by a switching device (to produce quasi -square waves), or by a non-linear resonant circuit (for example, a constant voltage transformer). The latter, because their operation requires driving part of their core into saturation, are less efficient than ordinary transformers of the same VA rating. Also they tend to pull spikes of current which requires overdesign of the inverter power stage. Although they provide inherent current limiting, the voltage regulation with load change is not adequate for these applications; thus, the constant voltage transformer was not felt to be suited for this application.

   Switching of the (a. c.) output to produce essentially a quasi-square wave would require an additional switch as shown in Figure 1-8 to provide zero clamping and avoid the unclamped waveform shown in Figure 5K.

In the absence of feedback, the input voltage variations will account for the greatest portion of the output voltage variation and will affect all three phases equally. The load variations on any one phase will affect that phase more than the other two.

The amount of interaction, if any, will depend on the design of the inverter. It is advantageous to have the three phases tied together as much as possible since with phase shift techniques (which are indicated here) it is simpler from the control point of view to vary all three phases simultaneously than individually.

Load sharing techniques basically involve using part of the output of one phase to make up the composite output of another phase. In this fashion a load on one output phase will result in some effective load being placed on at least part of the inverter stages for all phases. One method for doing this is to start with a two phase inverter and transform the outputs with a Scott-Tee, yielding a three phase output and two primary phases which are generally both loaded (though not equally) by a load on any one of the (three) secondaries. Another method is to start with a three phase inverter and wind three secondaries on each output transformer; these secondaries (which may be of different number of turns) are then each connected in series with others from different phase output transformers to yield a composite output. Depending on the relative number and phasing of the interconnected windings, different harmonics may also be cancelled out. For instance, in the case of the simplest three phase inverter, the switched output of which is simply three square waves, each 120° out of phase with respect to the others, the addition of the output of any one phase and half the inverted sum of the other two results in a composite wave which has no third harmonics.[8] The individual generated

waveforms (A, B, and C) along with the phase A composite output $A' = A + \frac{1}{2}(-B-C)$ appear in Figure 1-9; a circuit for generating three phase waveforms of this type is shown in Figure 10.

Algebraically, that the resultant contains no third harmonic can be seen as follows:

$$V_A = \frac{4V}{\pi}\left[\sin\theta + \frac{1}{3}\sin 3\theta + \frac{1}{5}\sin 5\theta + \cdots + \frac{1}{(2n+1)}\sin(2n+1)\theta\right]$$

$$V_B = \frac{4V}{\pi}\left[\sin(\theta-120^\circ) + \frac{1}{3}\sin 3(\theta-120^\circ) + \frac{1}{5}\sin 5(\theta-120^\circ) + \cdots + \frac{1}{(2n+1)}\sin(2n+1)(\theta-120^\circ)\right]$$

$$V_C = \frac{4V}{\pi}\left[\sin(\theta+120^\circ) + \frac{1}{3}\sin 3(\theta+120^\circ) + \frac{1}{5}\sin 5(\theta+120^\circ) + \cdots + \frac{1}{(2n+1)}\sin(2n+1)(\theta+120^\circ)\right]$$

$$V_A - \frac{1}{2}(V_B+V_C) = \frac{8V}{\pi}\left[\sin\theta + \frac{1}{5}\sin 5\theta + \cdots + \frac{1}{(2n+1)}\sin(2n+1)\theta\right] \quad \text{for } (2n+1) \neq \text{multiple of 3.}$$

(because for $(2n+1)=3k$ (k an integer) $\sin(2n+1)(\theta \pm 120^\circ) = \sin(2n+1)\theta$

Though providing cancellation of the largest and most troublesome harmonic, this technique is again wasteful of transformer capability and weight because:

1. The voltages added together in the secondaries are not all in phase, resulting in a smaller vector sum then algebraic sum and hence wasteful of transformers in the same fashion as the phase shift voltage regulation techniques already discussed.

2. Because the sum of the three square wave voltages applied to the phase output transformers does not equal zero, these three single phase transformers cannot be combined into a single three-phase transformer, (which would be smaller and lighter than the three single phase units.)

A scheme which avoids these objections (again at the expense of a more complex logic system) consists of 3 120° quasi-square wave drives, spaced 120°. Each individual power switch output is thus free from the third harmonic to begin with. Furthermore, each transformer now provides $\frac{\sqrt{3}}{2} \simeq .866$ of the fundamental output of a transformer operated at the same voltage with a square wave drive, but it only has to support $2/3 \simeq .67$ of the volt seconds as a transformer with square wave drive. Thus, it is more efficiently used. In addition, because the sum of the output voltages from this three phase switching system equals zero, a three phase output transformer can be used. Figure 1-11 shows the output voltages of the three phases of such a unit; inspection will show that the sum of these three voltages equals zero. The usual objection to the quasi-square wave switching stage, its need for extra switching elements to perform the zero clamping function, does not apply here if a three phase transformer is used as the output transformer because a glance at Figure 1-11 will show that there are always two and only two switches on at the same time, and they are producing equal and opposite voltages. Thus, the voltage in that winding which has neither side energized through a switch must be zero in order to satisfy the flux relations required of the core. Notice that if three single-phase transformers were used instead, this relationship would not need apply and some form of zero clamping would be needed for the switching stages.

To obtain voltage regulation with respect to input voltage and balanced load

variations, two waveforms produced by either of these techniques or any other suitable one can be added together with a voltage feedback controlled variable phase shift between them. The resulting summation wave also contains no harmonic not present in the individual waveforms and, depending on the spacing, may contain reduced amounts of other harmonics.

This method provides voltage regulation to compensate for input voltage and balanced load variations. The variation due to any unbalanced loads cannot be compensated by this scheme, since it cannot vary the output of one phase only. A further analysis of this circuit will indicate how much of a variation of output voltage with unbalanced load can be expected. This variation, which is expected to be fairly small, could then be accounted for by individual low power quasi-square wave regulators in series with each phase output.

Each quasi-square wave power stage would be controlled by a voltage feedback circuit sensing the output of the phase in which that quasi-square wave source was connected. By varying the width of the quasi-square wave over a wide range, the phase voltage would vary a smaller but adequate percentage. Should the inverter outputs have too large phase shifts from the 120° separation required, the phase of each individual quasi-square wave with respect to the main switched output voltage could be varied by a phase feedback network, to bring the overall phase displacement within specification. The block diagram for such a system is shown in Figure 1-12.

IV Conclusions

A survey of inverter configurations and switching devices was undertaken and representative inverter circuits analyzed. The 3200 cps 3Ø 10 Kw inverter was assumed to be the most difficult, and an effort was started to determine an optimum configuration for it by examining various inverter circuits in light of the special problems posed. It was felt that there were two basic design decisions to be made. One was the selection of the basic power switching stage and power switching element. The second is the technique of combining these basic elements to obtain a three phase, voltage regulated sinusoidal output. Though neither of these has been completed, the first has been investigated enough that the following rating charts can be made. On the basis of Table 1-1 which compares switching elements, it would appear that, depending on the temperatures the inverter would have to operate in, and the amount of thermal derating desired, either the silicon or germanium transistor would be chosen as the switching element.

Because the series inverter circuits are load sensitive and are also generally used with SCR's as opposed to the transistors indicated above, they are not feasible as the fundamental power switching stage for this inverter. The bridge circuits, with two semiconductors in the forward path of the d.c. input current have twice the losses and twice the number of semiconductors of the center-tapped primary type. Since the number of weight and losses added by these extra power switching elements will be greater than the

savings accrued through more efficient use of the output transformers, the use of any type of bridge circuit is contraindicated. Thus, the power switching stages shall be of the parallel inverter with center-tapped transformer primary type.

The various possible methods of voltage regulation are shown in Table 1-2 along with their advantages and disadvantages. These are for an output of 28 v nominal and an output of 115 volts. (This is mentioned because under different input and output conditions, the desirability of the different techniques will vary. For example, if the output voltage were only 6 volts, the technique of saturable reactor or SCR modulation of the output would be extremely inefficient. Similiarly, at higher input voltages and wider voltage variations, the efficiency of the d.c. regulator technique would be competitive with the others, while it is not at 28 v.)

On the basis of the material in this Table, it appears that the phase shift regulation is most advantageous for the 3200$\sim$10 Kw inverter. It allows high efficiency with a minimum of power semiconductors.

TABLE 1-1

Static Inverter Power Switch Rating Chart

(Units chosen for 3200~ operation @ 28+10 -20% input voltage)

DEVICE	GERMANIUM TRANSISTOR	SILICON TRANSISTOR	SILICON CONTROLLED RECTIFIER	GATE CONTROLLED SWITCH
PARAMETER				
Weight	Lightest	Medium (Silicon transistors and drive circuitry weigh more than germanium units)	Heaviest (due to commutating choke and capacitor)	Medium (Slightly heavier than Silicon Transistor unit because of extensive paralleling required)
Efficiency	Best (low forward loss medium switching loss low drive loss)	Fair (medium high forward loss medium switching loss high drive loss)	Fair (medium forward loss high commutating losses lowest drive loss)	Fair (high forward loss medium switching loss low drive loss)
Reliability	Allows least temperature derating. High parts count. Redundancies possible in paralleled circuits.	Allows greatest temperature derating. High parts count. Redundancies possible in parallel circuits.	Slightly more thermal derating possible than with germanium. Smallest parts count. Danger of circuit failure without component failure. No redundancy.	Same thermal derating as SCR's. Highest parts count (due to large amount of paralleling required.) Danger of circuit failure without component failure. Redundancy Possible.
Ease of High Power Operation	Fair, requires paralleling	Fair, requires paralleling	Excellent, very large units available	Poor, requires extensive paralleling
Max. Junction Temp. allowed by Manufacturer	110°C	200°C	125°C	125°C

Note: Weight and efficiency include losses and weight of all auxiliary equipment used (which varies depending on the switching device chosen.)

TABLE 1-2

Voltage Regulation Techniques

INVERTER → TYPE	INPUT REGULATORS	CONVERSION REGULATORS		OUTPUT REGULATORS	
	D. C. Regulator	Quasi-Square Wave	Phase Shift Regulation	Constant Voltage Transformer	Mag Amp or SCR Modulator, Static Tap Changing
Number of Power Semiconductors*	Approximately 1.5 x minimum. (The additional ones are required in the d. c. regulator)	Approximately 1.5 x minimum (The additional ones are required for zero clamping)	Minimum	Minimum	Minimum plus those required in the modulators
Relative Losses in Power Semiconductors	2	1	1	1	$1 + \frac{1}{\text{sec. to pri. turns ratio of output XFMR}}$
Output transformer utilization	Excellent: Minimum volt-second capabilities required; 3Ø XFMR usable	Good: Minimum volt-second capability required; 3Ø XFMR not usable	Good: Some volt-second capability wasted. 3Ø XFMR usable	Poor: Some volt-second capability wasted. 3Ø XFMR not usable	Good: Some volt-second capability wasted. 3Ø XFMR possible
Logic & Control	Power switching stage drive is simple. D.C. voltage regulator control and filter are required	Complex drive circuitry required.	Complex drive circuitry required, though simpler than for quasi-square wave generation.	No voltage control required. For unbalanced loads, phase separation must be feedback controlled.	Power switching stage drive is simple. Control similar to that used for quasi-square wave drive is also needed here.
Other	Can provide protection against input transients			Output voltage sensitive to load pwr factor	
Efficiency	Fair (at 28 VDC) due to added losses in regulator semiconductors	Good	Good	Poor, due to high transformer losses	Good

* This number is based on the assumption that some type of paralleling would be required in each case. Hence, it does not hold in the case of very low power inverters where, for example, only two transistors could supply the constant voltage transformer with the necessary power, but four (albeit smaller) to be needed for any phase-shift technique.

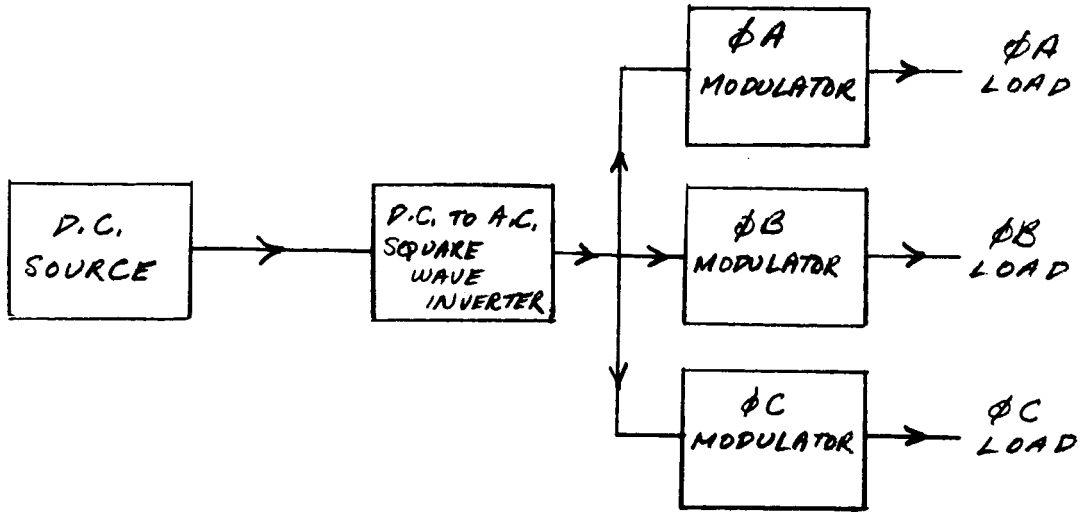


FIG. 1-1 POWER SECTION BLOCK DIAGRAM — THREE PHASE PULSE MODULATION INVERTER

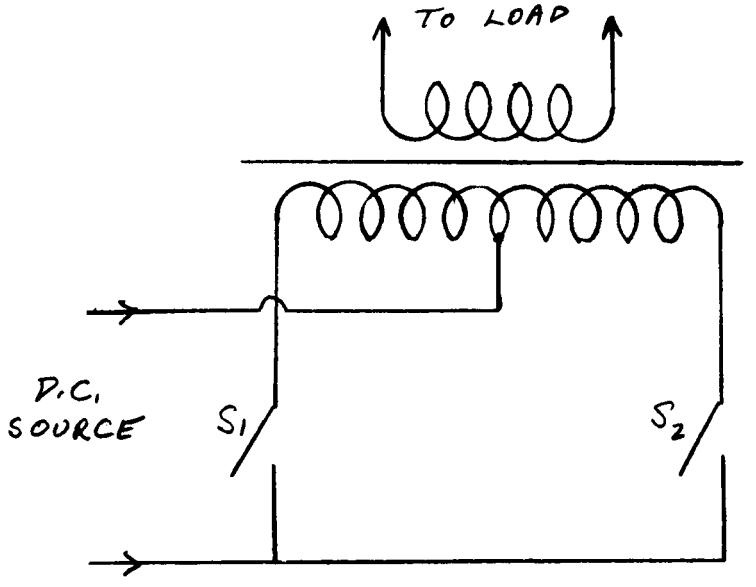


FIG. 1-2 SCHEMATIC OF TRANSISTORIZED SQUARE WAVE INVERTER

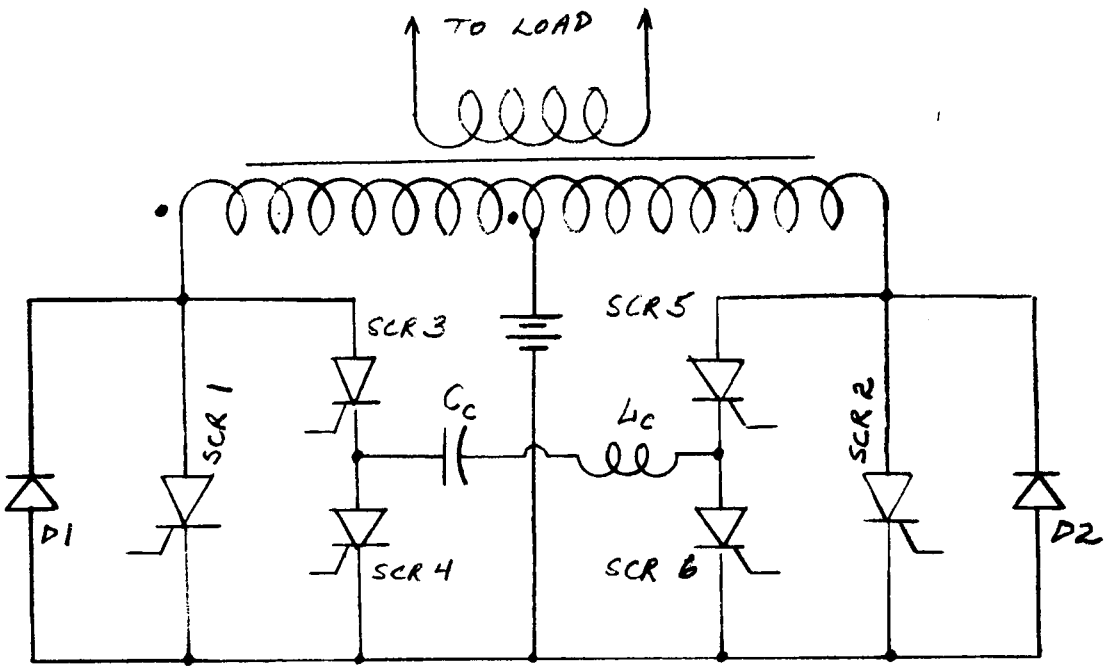


FIG. 1-4 MODIFIED PARALLEL INVERTER

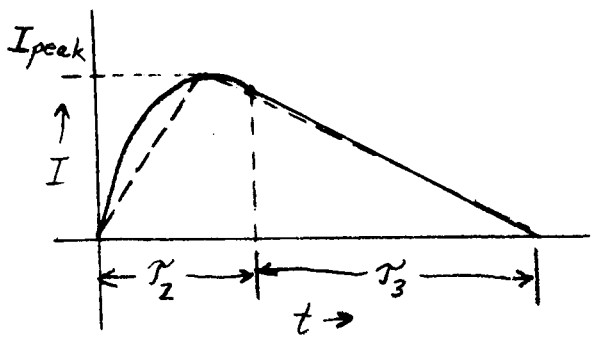


FIG 1-3 SCR CURRENT DUE TO COMMUTATION; McMURRAY-BEDFORD CIRCUIT

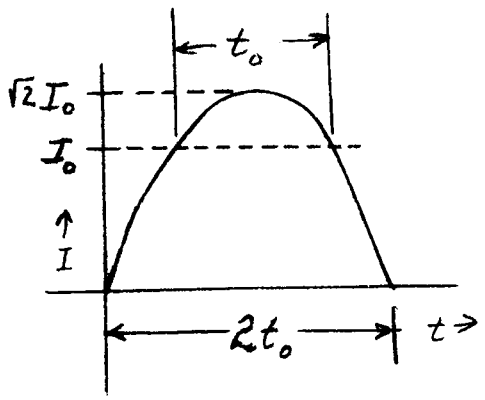


FIG 1-5 COMMUTATING SCR CURRENT; McMURRAY INV.

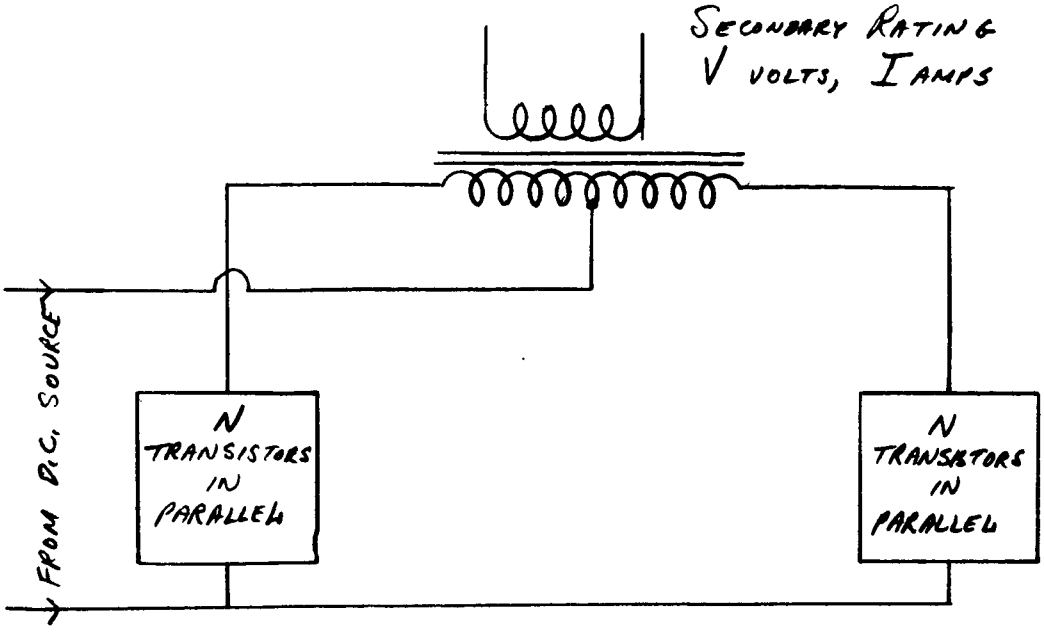


FIG. 1-7A CIRCUIT WITH PARALLELING ON PRIMARY SIDE

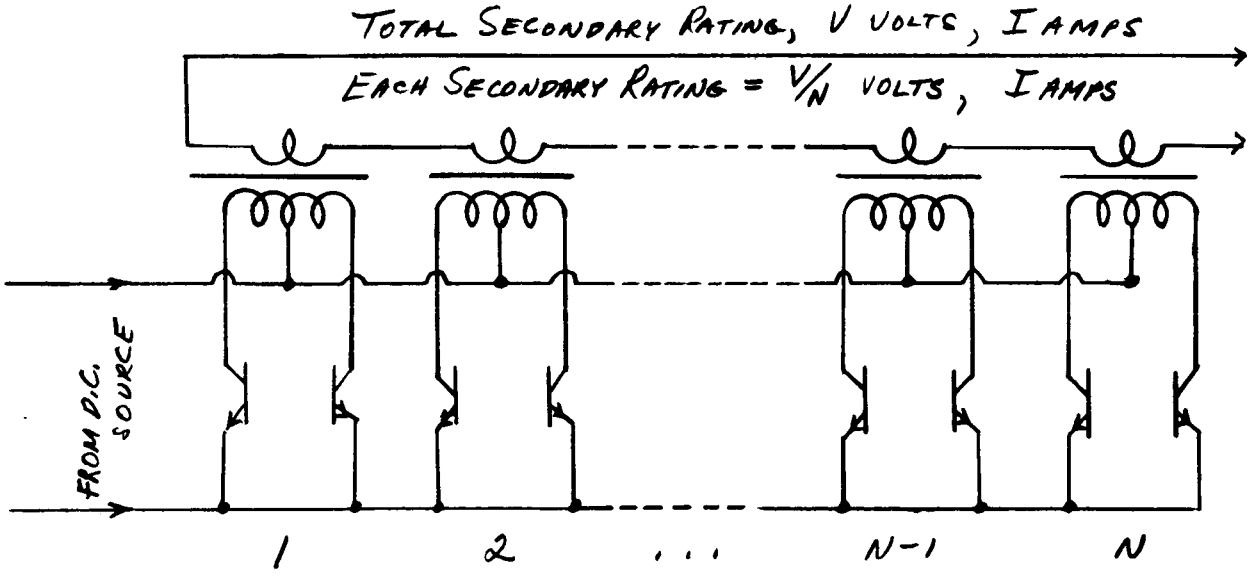


FIG 1-7B CIRCUIT FOR PARALLELING ON SECONDARY SIDE

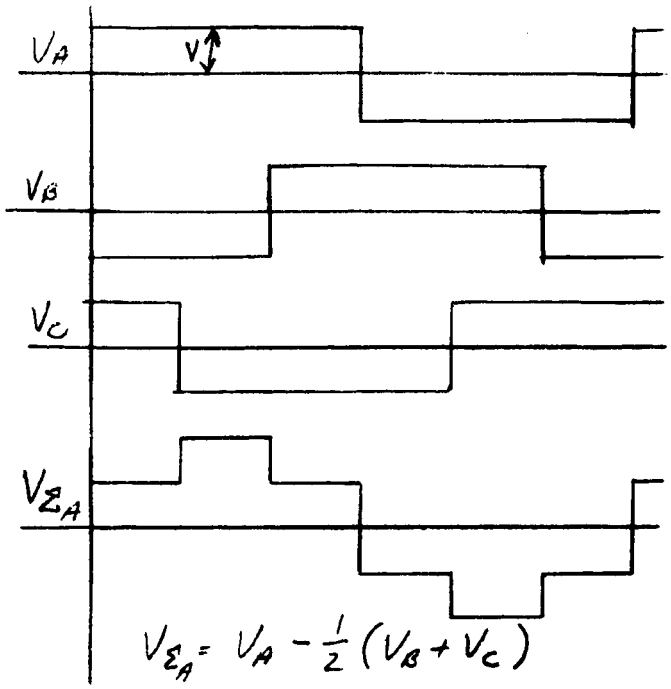


FIG. 1-9 HARMONIC REDUCTION AND LOAD-SHARING WAVEFORMS

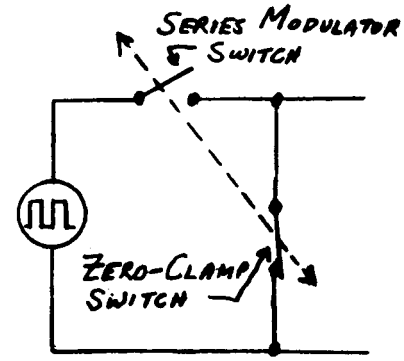


FIG. 1-8 OUTPUT MODULATOR ZERO-CLAMP TECHNIQUE

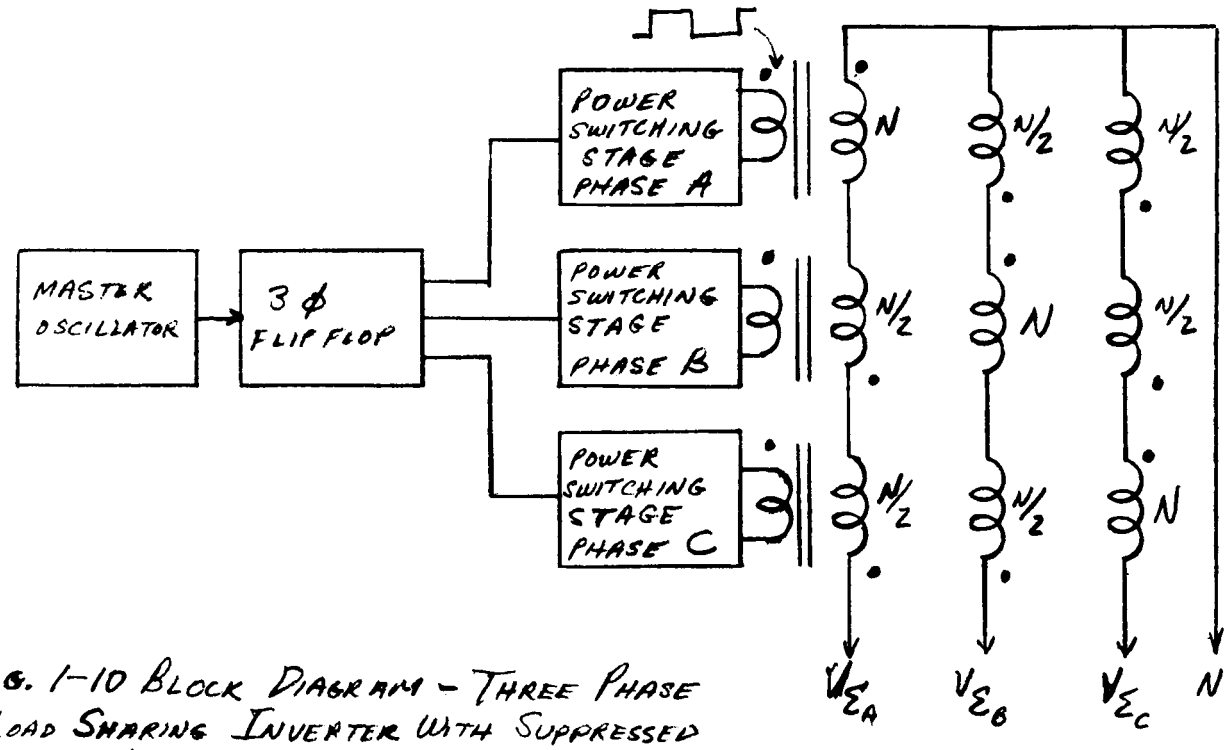


FIG. 1-10 BLOCK DIAGRAM - THREE PHASE LOAD SHARING INVERTER WITH SUPPRESSED THIRD HARMONIC

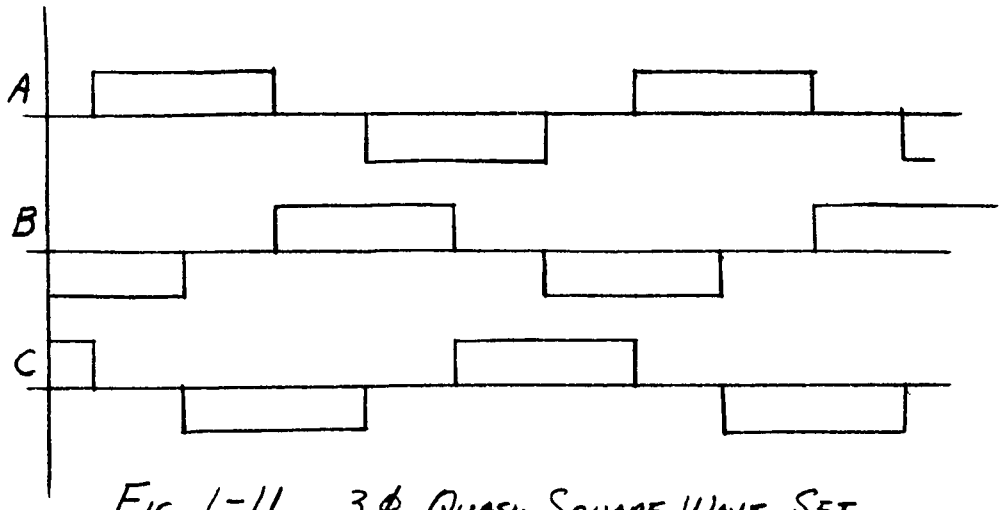
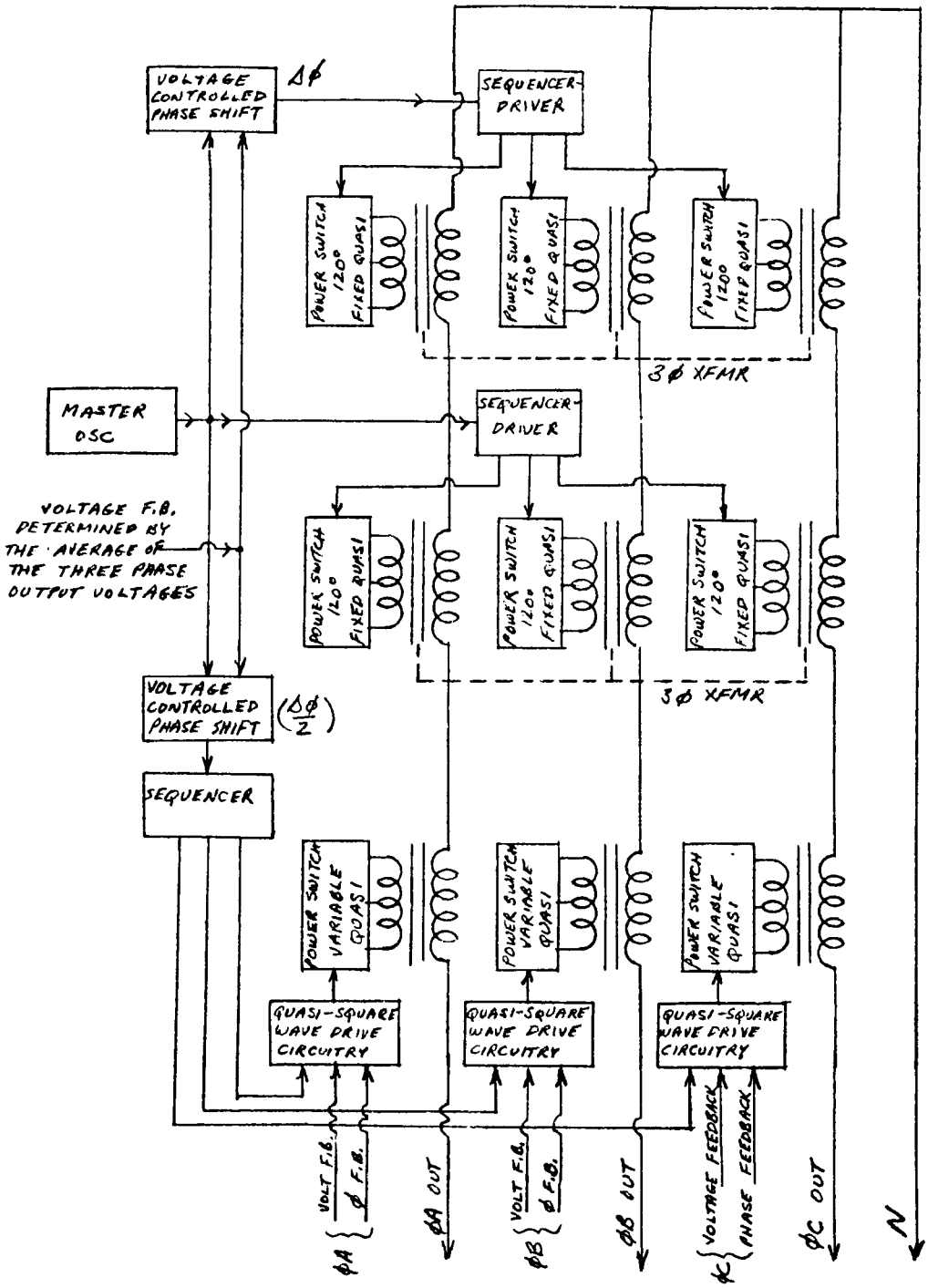


FIG. 1-11 3 ϕ QUASI-SQUARE WAVE SET

FIG. 1-12 3φ 3200W INVERTER BLOCK DIAGRAM



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